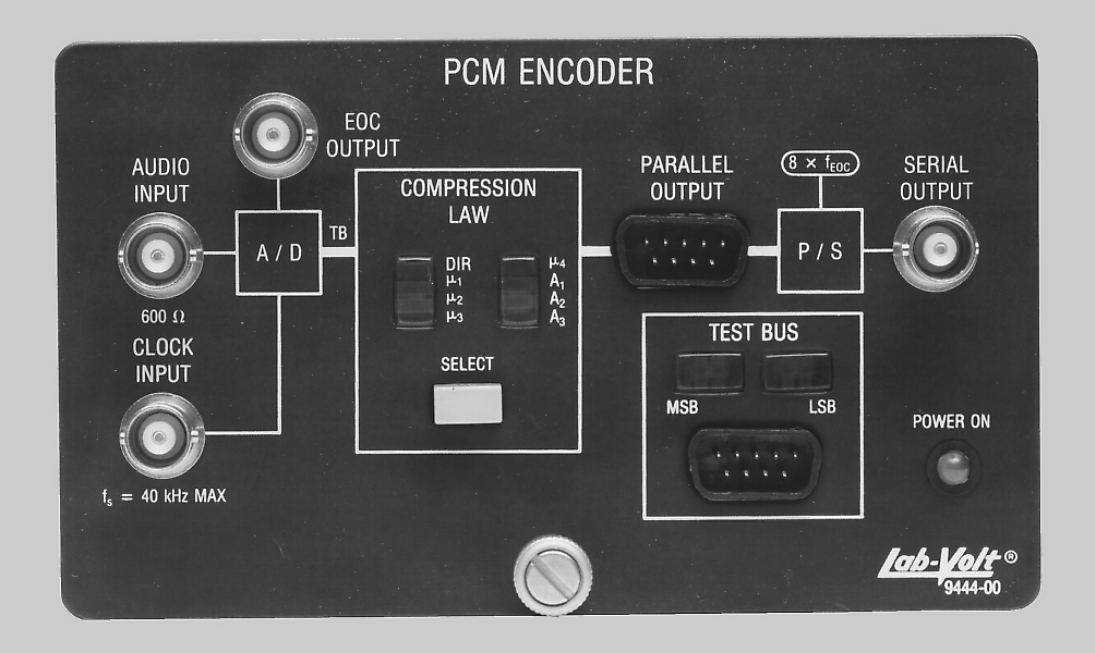
PCM Encoder

Model 9444

Instruction Manual



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INTRODUCTION

The PCM Encoder, Model 9444, is manufactured and tested under strict quality control. If the PCM Encoder requires repair within the warranty period, contact your field representative to obtain instructions for forwarding the module to the nearest authorized Lab-Volt Service Center.

If the PCM Encoder requires repair after the warranty period, it is recommended that it be returned for service.

Note: *The technical information and diagrams in this instruction manual were up to date at the time of publication. It is possible, however, that modifications have since been made in order to improve the product. To have the most up-to-date information, contact your field representative and state both the model and serial numbers.*

Note: *This equipment is for use only in industry and school laboratories where qualified supervision is provided.*

WARRANTY

Lab-Volt warrants all equipment against defects in material and workmanship for a period of one year from the date of installation and/or acceptance by the customer. This warranty covers only the intended use of the equipment and does not cover damage due to alteration, negligent use or normal wear.

We assume no liability for damage, injury or expense claimed to have been incurred through the installation or use of our products.

Questions concerning this warranty and all requests for repairs should be directed to the Lab-Volt field representative in your area.

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SECTION 1

DESCRIPTION

The PCM Encoder, Model 9444, part of the Lab-Volt Digital Communications Training System, has been designed for the Study of pulse-code modulation (PCM). The PCM Encoder converts an analog signal into a series of digital coded words.

For this, the PCM Encoder uses an analog-to-digital (A/D) converter. The A/D converter takes samples of an analog signal and converts them into 8-bit words. A clock signal determines the rate at which the conversion is carried out. A LED display called TEST BUS allows the 8-bit words at the output of the A/D converter to be observed when a very-low frequency analog signal is sampled.

A digital compressor allows each of the 8-bit words coming from the A/D converter to be compressed. Compression is a technique used in order to increase the signal-to-noise ratio of the PCM system for the transmission of low level analog signals. A push button allows the selection of the compression law (μ_1 to μ_4 and A_1 to A_3) used by the digital compressor.

Finally the PCM signal can be transmitted in parallel or serial form. A multi-pin connector provides the parallel-form PCM signal. For serial-form transmission, a parallel-to-serial (P/S) converter converts the parallel-form PCM signal into a serial-form PCM signal. A BNC connector provides the serial-form PCM signal.

Fault switches located inside the module allow fault insertion. The BNC terminals and the multi-pin connectors on the front panel of the module allow troubleshooting or analysis of the system through the observation of signals at various stages in the circuit.

The PCM Encoder, Model 9444, has been designed to be inserted into the Enclosure / Supply Regulator, Model 9420. Regulated power is provided through the backplane connectors of the Enclosure / Supply Regulator mating with the edge connector on the back of the PCM Encoder. The inputs and outputs of the module are protected against all misconnections and short circuits. A thumb screw securely fastens the module to the Enclosure / Supply Regulator.

SECTION 2

SPECIFICATIONS

Power Requirement . . . . . +15 V –60 mA
+5 V –190 mA
–5 V –2 mA
–15 V –40 mA

Audio Input
- Impedance . . . . . 600 Ω
- Maximum Level* . . . . . ±1 V
- Maximum Frequency . . . . . ~½ clock frequency

Clock Input
- Level . . . . . TTL
- Maximum Frequency . . . . . 40 kHz
- Active Transition (indicating start of conversion) . . . . . Positive

EOC Output
- Level . . . . . TTL
- Frequency . . . . . 1 pulse / conversion
- Active Transition (indicating end of conversion) . . . . . Positive

Serial Output
- Level . . . . . TTL
- Bit Rate 8 x EOC-signal frequency
- Minimum Bit Rate . . . . . 2400 bits/s
- Maximum Bit Rate . . . . . 320 kbits/s

Parallel Output
- Level . . . . . TTL
- Code
  - Without Compression . . . . . Offset
  - With Compression . . . . . Signed

Test Bus Output
- Level . . . . . TTL
- Code . . . . . Offset

A/D Converter Conversion Time** . . . . . 18 µs ±1 µs

Fault switches 8

Test Bus 1

*Maximum level in order to avoid distortion

**Time elapsed between the rising egde of the clock signal (start of conversion) and the rising egde of the EOC signal (end of conversion).

> **Note:** *This equipment must be powered with the Enclosure / Supply Regulator, Model 9420.*

SECTION 3

OPERATING INSTRUCTIONS

1 AUDIO INPUT – This BNC connector is used to inject an analog signal at the input of the A/D converter.

2 EOC OUTPUT – This BNC connector provides the EOC signal. When this signal is at logic level 0, a conversion is under way. When it is at logic level 1, the conversion is completed and a stable PCM signal is available at the PARALLEL OUTPUT.

3 PARALLEL OUTPUT – This nine-pin connector provides the processed PCM signal. Its pin configuration is given in Figure 1.

4 SERIAL OUTPUT – This BNC connector provides the processed PCM signal, in serial form. The most significant bit (MSB) comes out first.

5 POWER ON indicator – This green LED lights when power is correctly applied to the module.

6 TEST BUS output – This nine-pin connector provides the PCM signal coming from the output of the A/D converter. Its pin configuration is given in Figure 1

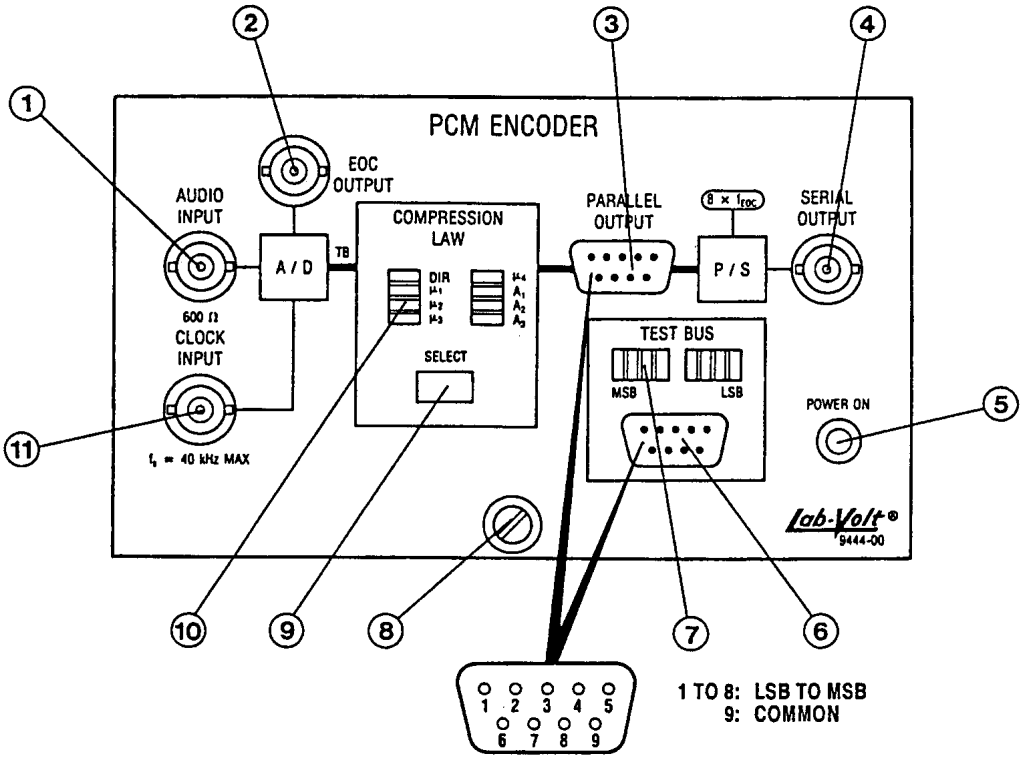

Figure 1. Front Panel of the PCM Encoder.

7 TEST BUS display – This LED display indicates the logic level of each of the eight bits at the output of the A/D converter. A bit is at logic level 1 when the corresponding LED is lit and vice versa.

8 THUMB-SCREW FASTENER – It secures the module to the enclosure.

9 SELECT – This push button allows the transfer function of the digital compressor to be selected.

10 COMPRESSION LAW display – This LED display indicates the transfer function selected for the digital compressor.

11 CLOCK INPUT – This BNC connector is used to inject a clock signal which determines the rate at which the A/D conversion is being carried out.

SECTION 4

DESCRIPTION OF OPERATION

Figure 2 shows the block diagram of the PCM Encoder. The PCM Encoder consists mainly of an 8-bit A/D converter. An input amplifier multiplies the audio input voltage by about 10. After conversion by the A/D converter, the resulting 8-bit word is sent to the TEST BUS output (TB) and to the compression law ROM (digital compressor).

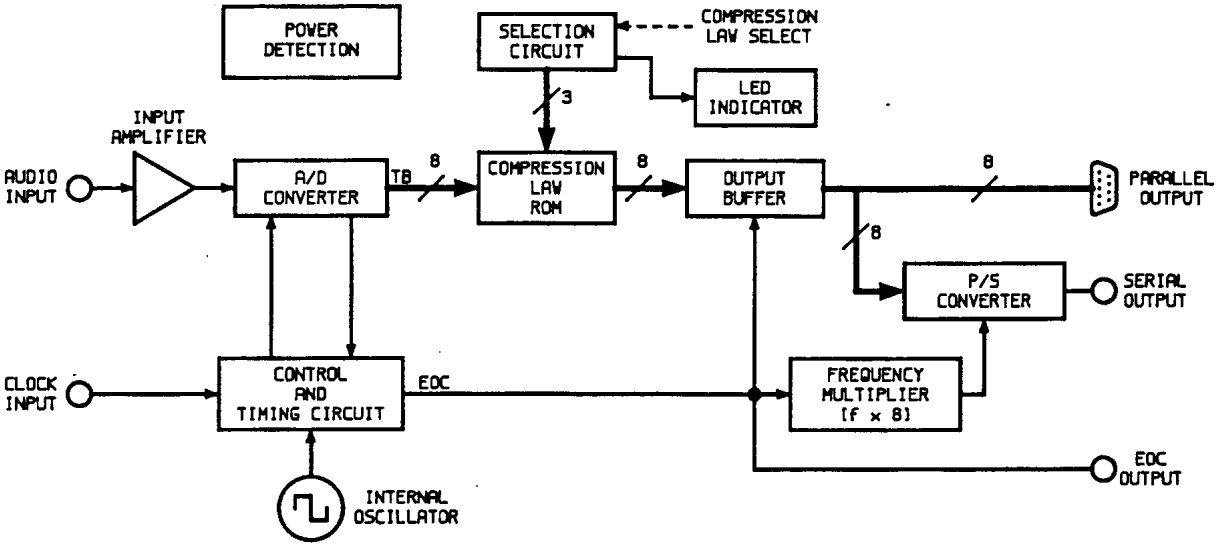

Figure 2. Block Diagram of the PCM Encoder.

The ROM is used for the digital compression of each 8-bit word at its input to a fewer-bit output word. The ROM contains 7 compression laws and a linear transfer function (DIRect mode). Either of these can be chosen by the selection circuit which also controls the LED indicator.

Each of the 8-bit words coming from the ROM is memorized by the output buffer before reaching the PARALLEL OUTPUT, and the parallel input of the P/S converter. The P/S converter sequentially shifts towards the SERIAL OUTPUT each of the 8-bit words coming from the output buffer – starting with the MSB. The P/S converter requires a clock signal whose frequency is 8-times that of the conversion clock signal to operate. A frequency multiplier produces this clock signal using the EOC signal.

SECTION 5

FAULT SWITCHES AND TEST BUS

5.1 Fault Switches

Fault switches enable the instructor to simulate faults for the teaching of troubleshooting. Access is through an opening in the transparent cover of the module. A fault is active when its corresponding switch is in the position I.

5.2 Fault Description

FLT 1 The gain of the input amplifier is reduced from ten to closer to five.

FLT 2 The positive reference voltage of the A/D converter is changed, causing it to clip the negative part of the audio signal.

FLT 3 The EOC signal is not present at the EOC OUTPUT.

FLT 4 The clock signal is not connected to the control and timing circuit, preventing the output of any signal.

FLT 5 The bits sequence at the SERIAL OUTPUT is logically inverted. The switch connects the inverted output of the P/S converter to BNC connector causing the recovered signal at the PCM Decoder to be inverted.

FLT 6 The frequency multiplier is disabled. Then, there is no signal at the serial output.

FLT 7 The MSB at the A/D converter output is replaced by the LSB.

FLT 8 The LSB at the A/D converter output is replaced by the MSB.

5.3 Test Bus

The test bus appearing on the front panel is identified below.

TB1 A/D Converter Output

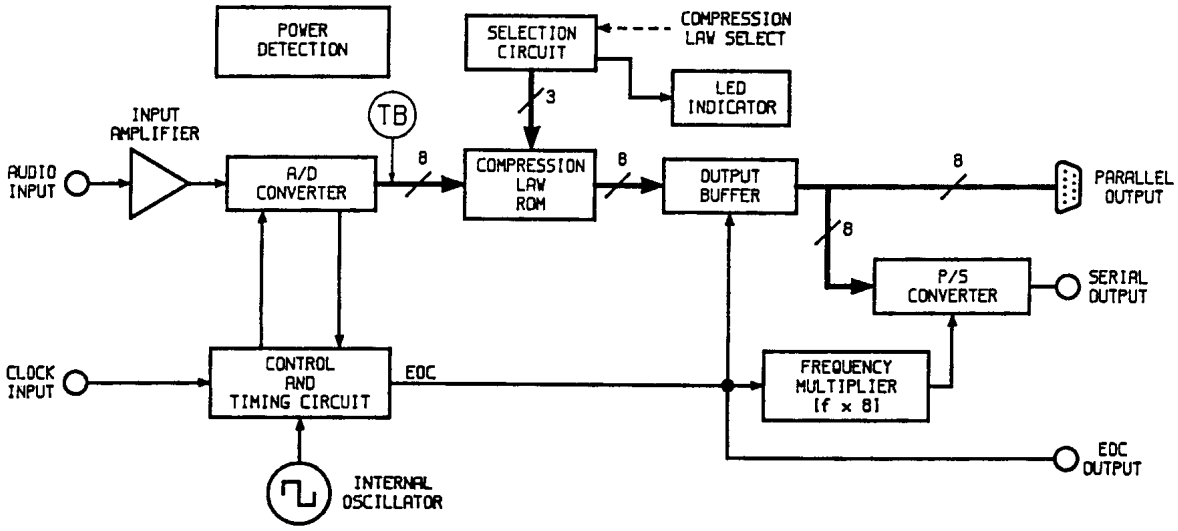

Figure 3. Location of the Test Bus.

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