Physical Limitations of Op Amps

- The IC Op-Amp comes so close to ideal performance that it is useful to state the characteristics of an ideal amplifier without regard to what is inside the package.

    – Infinite voltage gain

    – Infinite input impedance

    – Zero output impedance

    – Infinite bandwidth

    – Zero input offset voltage (exactly zero output voltage if input voltage is zero).

DC Imperfections

Three DC Imperfections of Real Op-Amps
Input Bias Current; Input Offset Current; and Input Offset Voltage
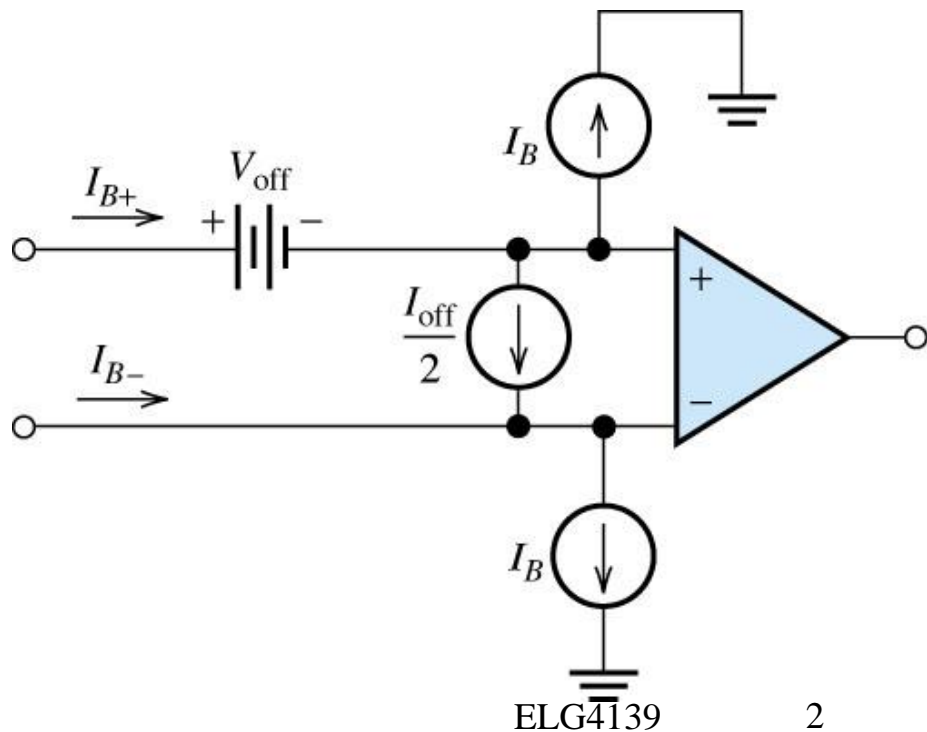(output voltage may not be zero for zero input voltage)

Bias Current: All Op-Amps draw a small constant DC bias currents at their inputs. Typical value for a 741 is around 100 nA. This is only notable when very high impedance sources are used. In such cases, an alternative op-amp with lower bias current should be used.

Bias Current

$$I_B = \frac{I_{B+} + I_{B-}}{2}$$
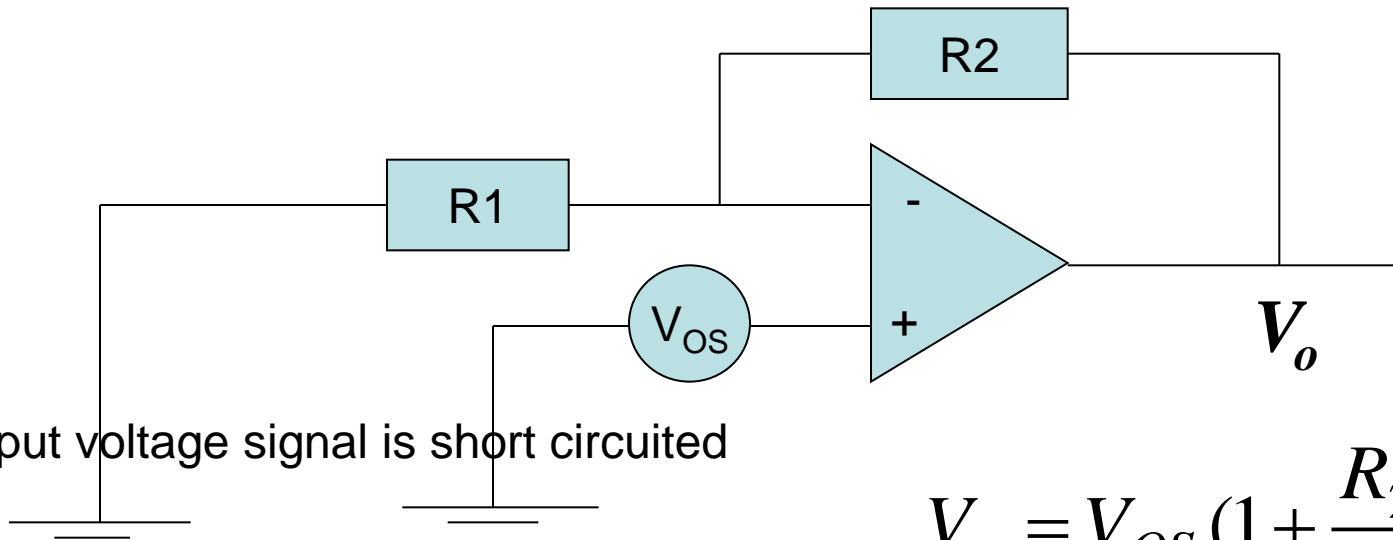
Offset Current

$$I_{off} = I_{B+} - I_{B-}$$

Offset Voltage

- When both input voltages are equal, the output should be zero. Actually it probably won't be due to an offset voltage between the inputs. Typically, this is around 2 mV.

- Offset voltage is automatically compensated by a negative feedback network. It can be a problem for precision comparator applications.

- Both the offset voltage and bias current are DC. A.C. operation is not affected by them (they just add an offset) Negative feedback reduces the effect of both. Steps can be taken to reduce them (further reading)

Observation

- Build any Op Amp circuit, apply zero voltage to its input, and what do you expect at the output?

- Although you would expect zero voltage, there is actually an error voltage present at its output.

- What causes this error? You can trace the error back to a number of unbalances in the Op Amp's internal transistors and resistors. To account for this in a circuit design, the net error is **modeled** as an offset voltage, V_{OS}, in series with Op Amp's input terminals.

- How will it affect the circuit? That depends on the Op Amp itself and the circuit design.

- The input offset voltage can range from µV to mV and can be either polarity.

- Bipolar op amps have lower offset voltages than JFET or CMOS types.

- The offset voltage is modeled in series with one of the op amp input terminals. Which one?

- Although the net effect is the same at either input, it is much easier to analyze V_{OS} in series with the non-inverting input. Why? The resulting circuit with V_{OS} at V+ looks just like the **non-inverting amplifier** configuration.
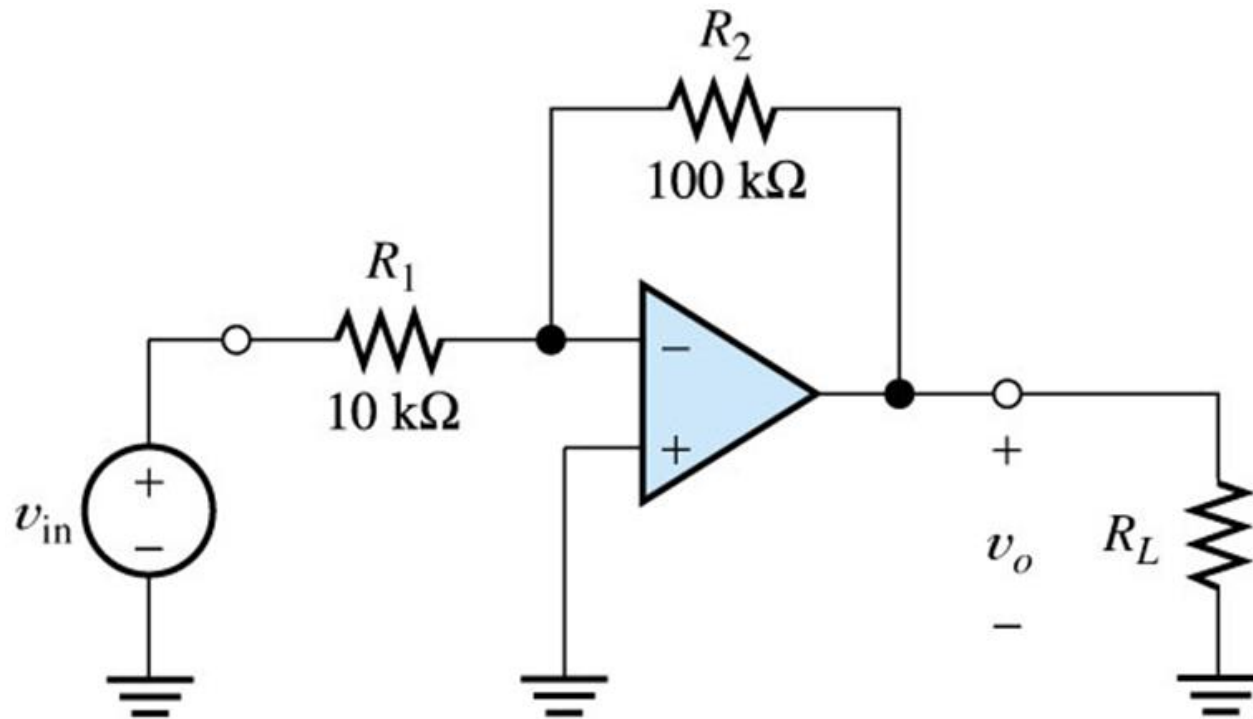
R2

R1

-

V_{OS}

+

V_o

The input voltage signal is short circuited

$$V_o = V_{OS}(1 + \frac{R_2}{R_1})$$
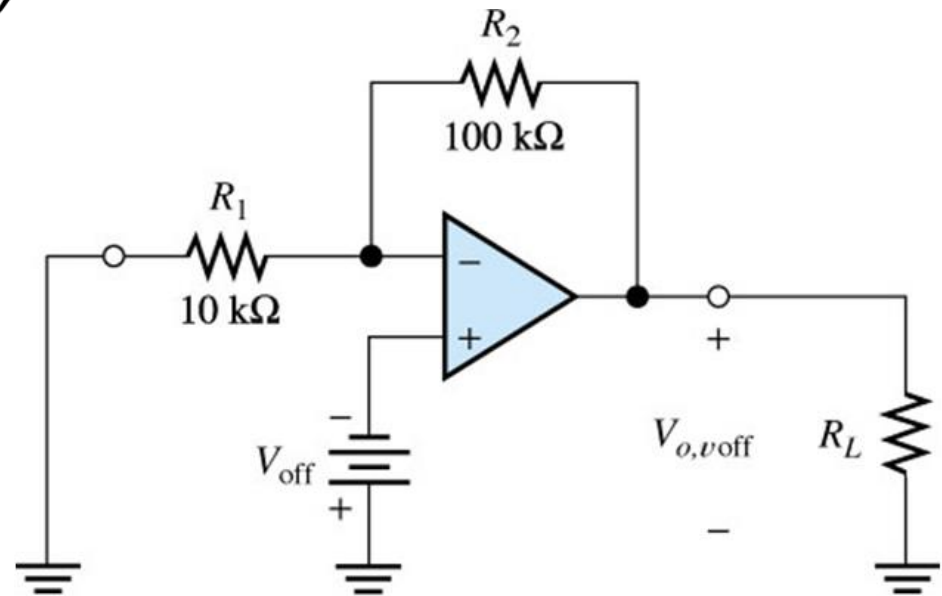
Actual op amp

-

+

- +

V_{OS}

Offset free op amp
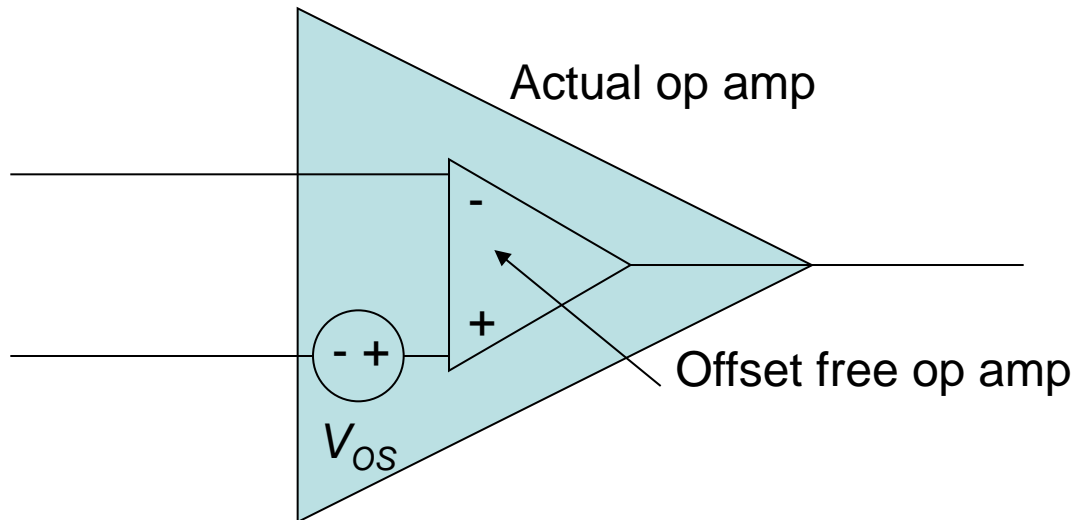
Example: Find the worst-case DC output voltage of an inverting amplifier assuming $v_{in} = 0$. The maximum bias current of the Op-Amp is 100 nA. The maximum offset current is 40 nA, and the maximum offset voltage is 2 mV.

First, Offset Voltage

$$V_{0,voff} = -\left(1 + \frac{R_2}{R_1}\right)V_{off}$$

$$V_{0,off} = -11V_{off}$$

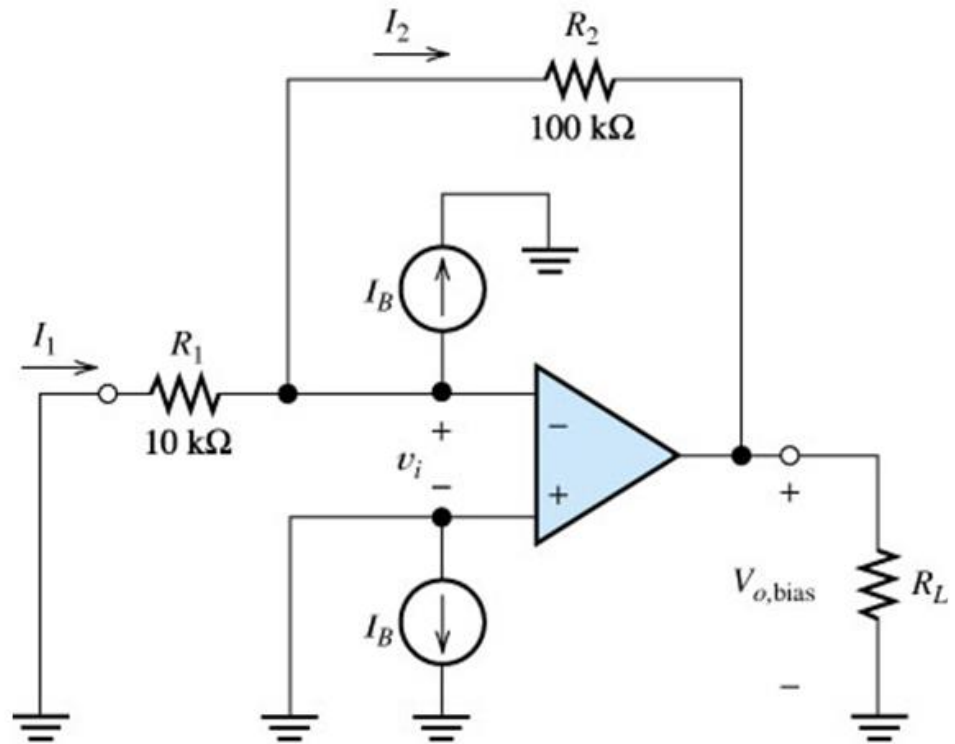$$V_{0,off} = -22 \text{ and} + 22\text{mV}$$

Second, Bias Current Sources
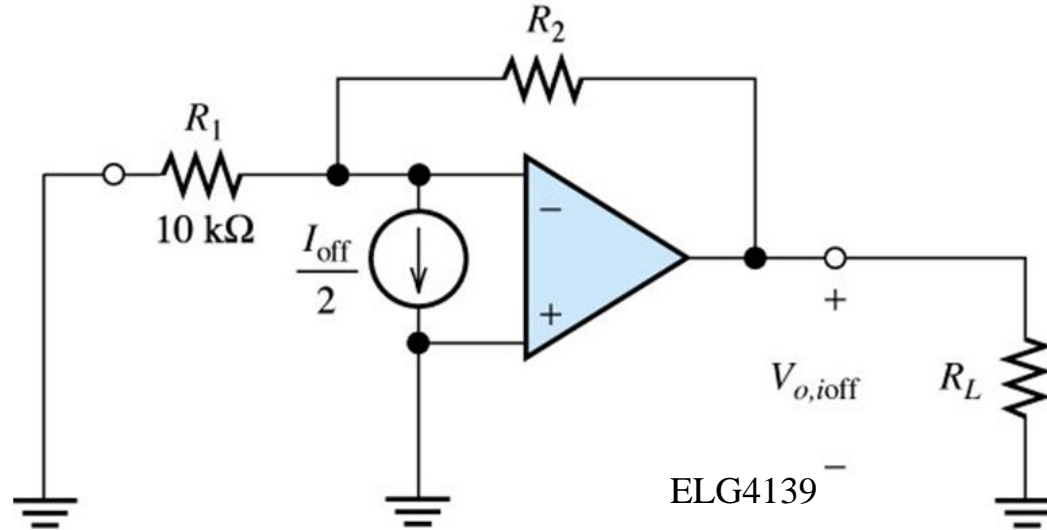
- $V_{0,bias} = -R_2 I_2 - R_1 I_1$

- $I_1 = 0$

- $I_2 = -I_B$

- $V_{0,bias} = R_2 I_B$

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Third, Offset Current Source

- $V_{0,ioff} = R_2\left(\dfrac{I_{off}}{2}\right) = $ -2 and 2 mV

- $V_0 = V_{0,voff} + V_{o,bias} + V_{o,ioff}$

- $V_0 = 22 + 10 + 2 = 34\text{mV}$

- $V_0 = -22 + 0 - 2 = \text{-24mV}$

Input Bias Current Compensation

- One of the practical op amp limitations is that the input bias currents for the two inputs may be slightly different.

- Even though the inputs are designed to be symmetrical, slight differences which occur in the manufacturing process may give slightly different bias currents.

- This offset current is typically on the order of a tenth of the input bias current, with 10 nA being a representative offset current for a 741 op amp.

- Even with identical source impedances, this offset current will produce a slight voltage between the input terminals, contrary to the ideal op amp.

R_2

$I_{B1} - I_{B2}R_3/R_1$

$I_{B2}R_3/R_1$

R_1

0 V

-

I_{B1}

I_{B2}

R_3

+

I_{B2}

V_o

$I_B = \dfrac{I_{B1} + I_{B2}}{2}$
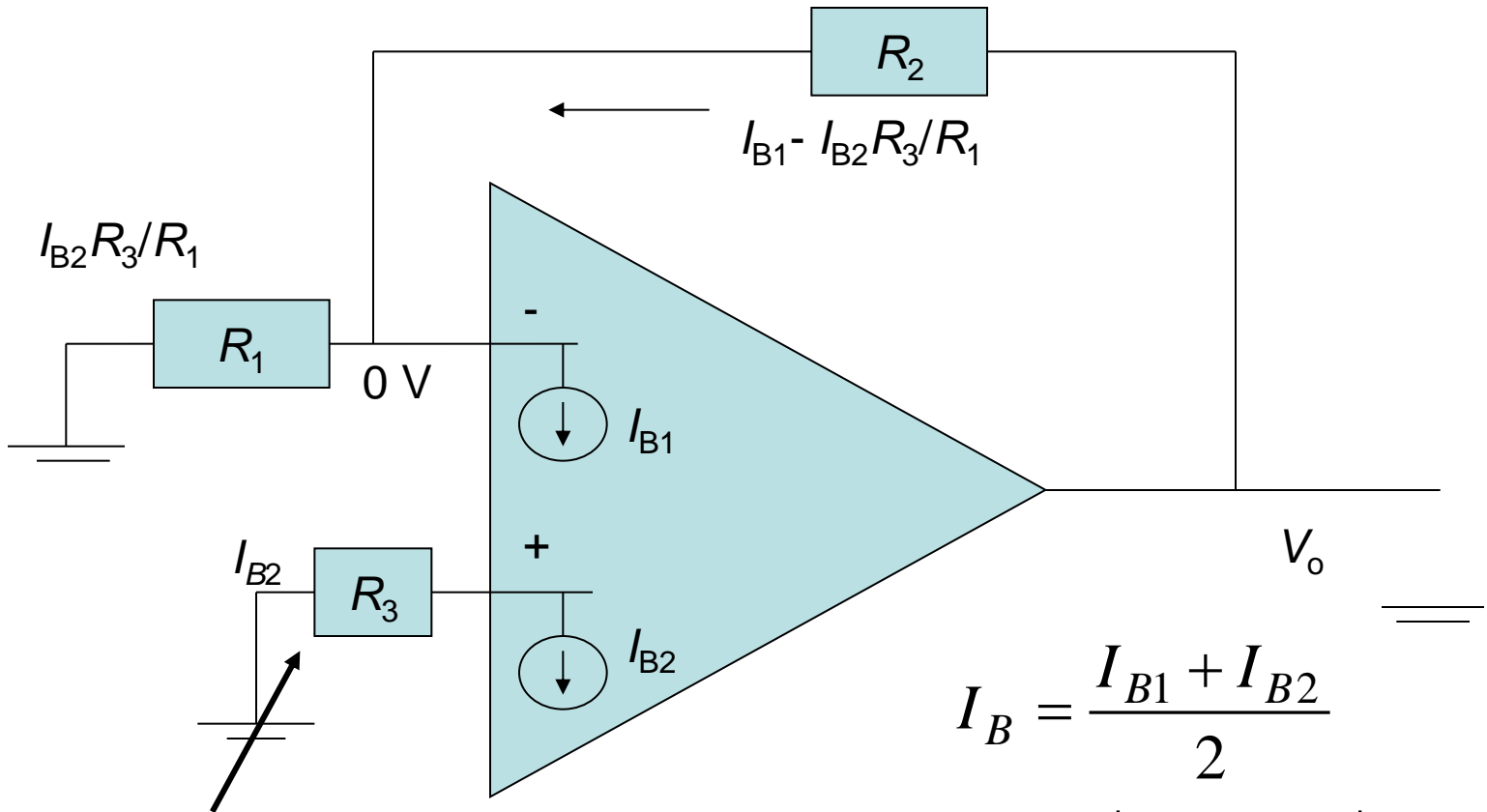
$I_{OS} = |I_{B1} - I_{B2}|$

A resistor may be added in series with the
Non-inverting input lead to reduce the value of
The output dc voltage due to input bias currents

$V_o = I_{B1}R_2 \approx I_B R_2 \text{ (no } R_3)$

$V_o = I_{OS}R_2 \text{ (with } R_3)$

$R_3 = \dfrac{R_1 R_2}{R_1 + R_2}$

- To minimize the effect of the input bias currents one should place in the positive lead a resistance equal to the DC resistance seen by the inverting terminal.

- If the amplifier is AC coupled, we should select $R_3 = R_2$.

- We must always provide a DC path between each of the input terminals of the op amp and ground. If we couple both input of the amplifier then the circuit will not operate without the resistance R_3 to ground.

Example: Consider an inverting circuit designed using an op amp and two resistors, R_1 = 10 kΩ and R_2 = 1 MΩ. If the op amp is specified to have an input bias current of 100 nA and an input offset current of 10 nA, find the output DC offset voltage resulting and the value of resistor R_3 to be placed in series with the positive input lead in order to minimize the output offset voltage. What is the new value of Vo.

$$V_O = I_B R_2 = 100\,\text{nA} \times 1\,\text{MΩ} = 0.1\,\text{V}$$

$$R_3 = \frac{R_1 R_2}{R_1 + R_2} = 9.9\,\text{kΩ} \approx 10\,\text{kΩ}$$

$$V_O = I_{OS} R_2 = 10\,\text{nA} \times 9.9\,\text{kA} \approx 0.01\,\text{V}$$

Offset Voltage Compensation

- In many applications, especially those for which the input signal is large compared to the offset voltage V_{OS}, the effect of the offset voltage is negligible.

- However, there are situations in which it is necessary to compensate for or null out the offset voltage.

- Two such methods are:
  - **Offset null terminals:** Some op amp are provided with two additional terminals to which a specified circuit can be connected to trim to zero the output DC voltage due to V_{OS}.
  - Offset compensation circuit through two terminals.
  - Capacitively coupling the amplifier.
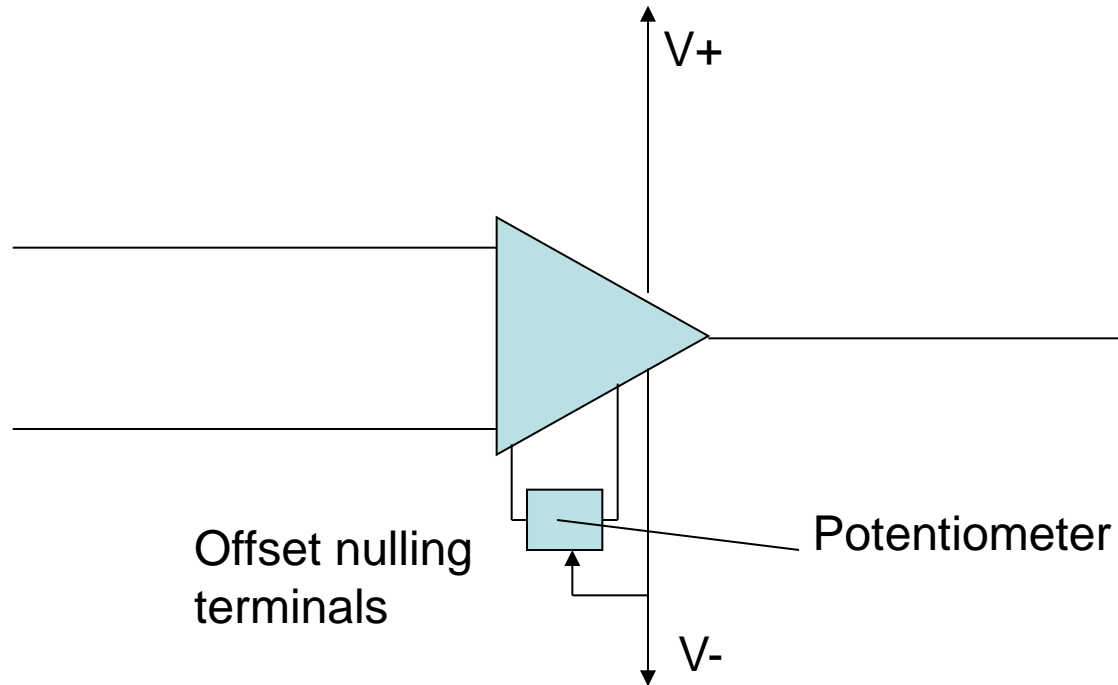
The output DC offset voltage of an op amp can be trimmed to zero by Connecting a potentiometer to the two offset-nulling terminals. The wiper Of the potentiometer is connected to the negative supply of the op am.
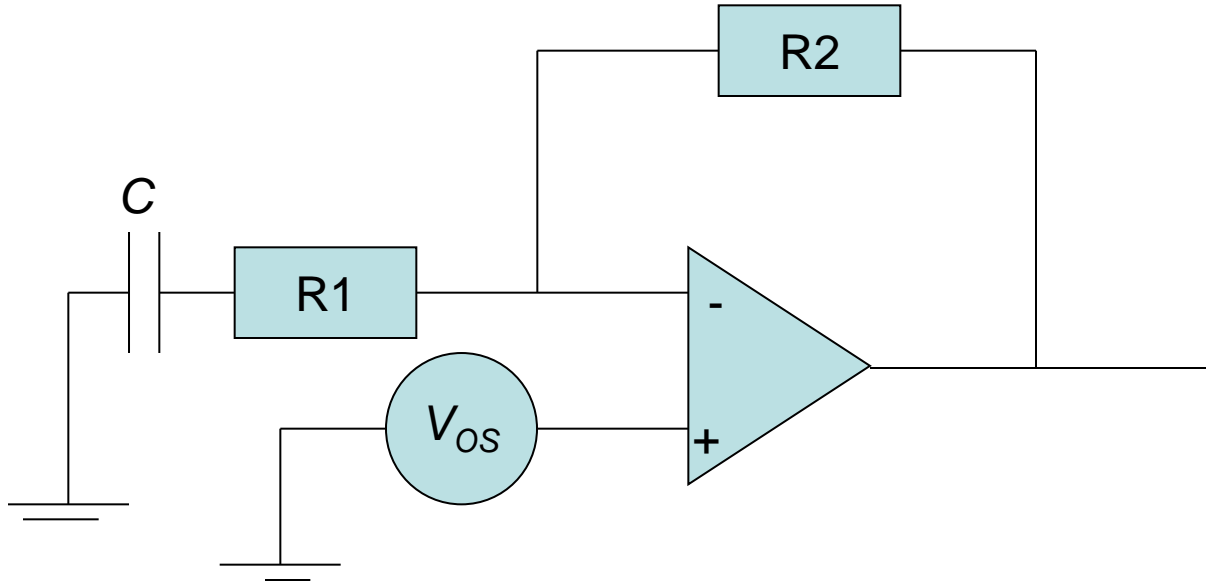
Capacitively coupled inverting amplifier.

Exercise: Consider an inverting amplifier with a nominal gain of 1000 constructed from an op amp with an input offset voltage of 3 mV and with output saturation levels of ±10 V. (a) What is the peak sine-wave input signal that can be applied without output clipping? (b) If the effect of V_{OS} is nulled at room temperature (25 oC) how large an input can now one apply if: (i) the circuit is to operate at a constant temperature? (ii) the circuit is to operate at a temperature in the range 0ºC to 75 ºC and the temperature coefficient of V_{OS} is 10 μV/ºC?

$$V_O = V_{OS}\,(1+\frac{R_2}{R_1}); \quad V_O = 3\text{mV}(1+1000) = 3\text{ V}$$

Maximum amplitude of a sine wave at the op amp output is $10 - 3 = 7\text{V}$.

(b) For part (i) $= 10\text{ mV}$

(b) For part (ii) : Temperature range of 0^OC to 75^OC corresponds to input offset

voltage range of $(0-25)\times10\mu\text{V} = \text{-}250\mu\text{V}$ to $((75-25)\times10\mu\text{V} = 500\mu\text{V}$.

This input offset range corresponds to output DC levels of

$-250\mu\text{V}(1+1000) = \text{-}0.25\text{ V}$ to $500\ \mu\text{V}\ (1+1000) = 0.5\text{ V}$.