Chapter 7

DC/DC CONVERTERS

DC/DC converters are the most common type of power conversion circuit. They change one DC voltage (usually unregulated) to another DC voltage (usually regulated). Many DC/DC converters are embedded within AC/DC power supplies.
Even most AC/DC power supplies consist of a diode bridge to change the AC input voltage into an unregulated high voltage DC followed by a DC/DC converter to produce a regulated, low voltage DC output.

7.1 BUCK CONVERTER (also known as a Buck Regulator)

The basic schematic circuit diagram for a Buck Converter is shown in **Figure 7.1**.

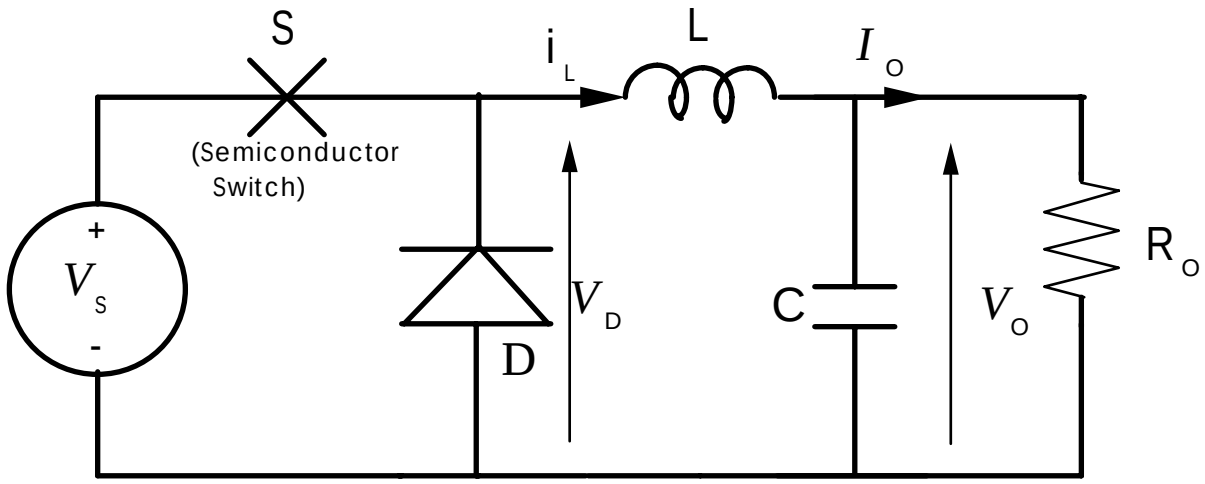


Figure 7.1 Basic Schematic Diagram for a Buck Converter

Switch S is turned on for t_1 seconds and then turned off for t_2 seconds such that:

$$t_1 + t_2 = T \qquad (7.1\text{-}1)$$

where T is the period for one switching cycle. The basic waveforms are shown in **Figure 7.2**

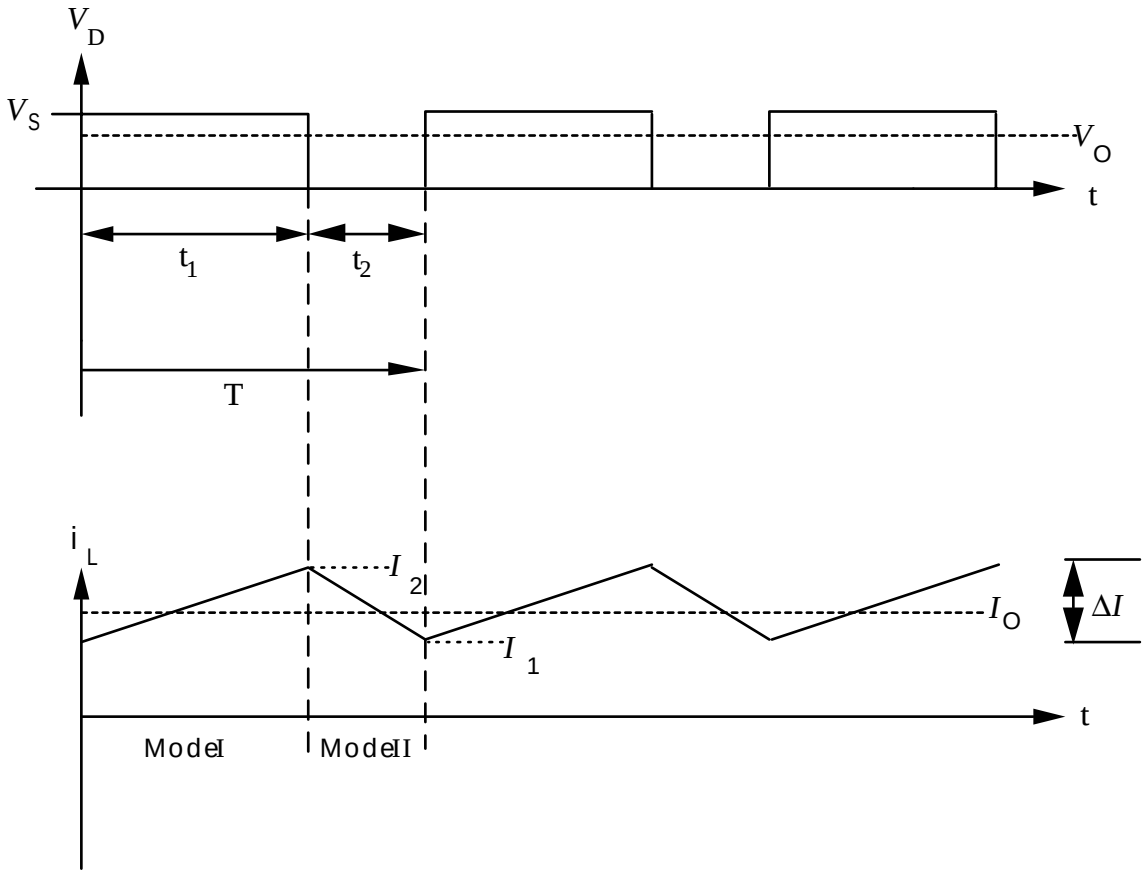


Figure 7.2 Basic Waveforms for the Buck Converter

We can assume that the output capacitor C is large enough such that V_O is constant and therefore I_O is also constant during the switching period.

When the switch S is turned on at $t = 0$, diode D becomes reverse biased and acts as an open circuit. This is referred to a Mode I and the equivalent circuit for this mode is shown in **Figure 7.3**.

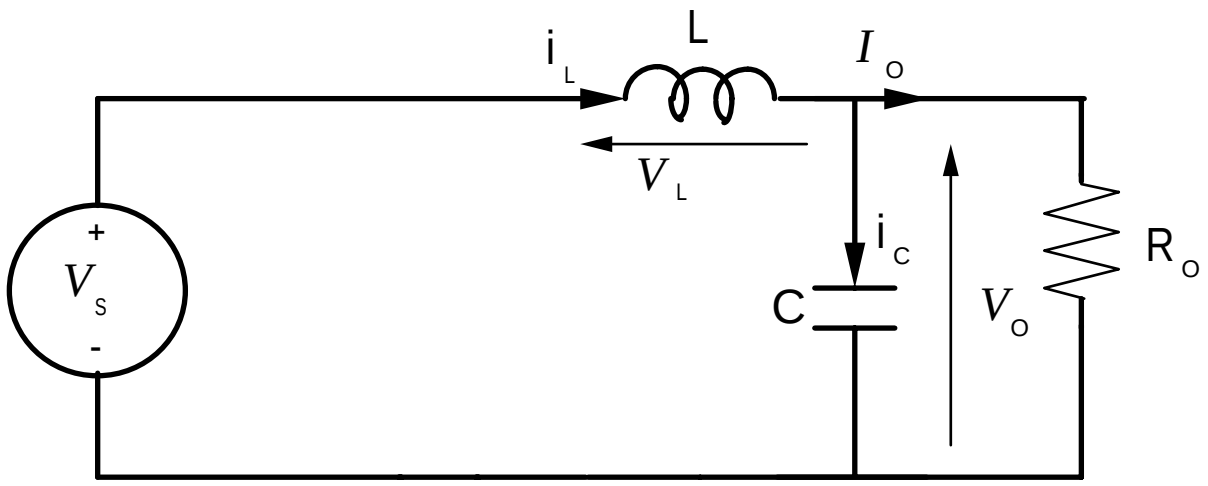


Figure 7.3 Basic Schematic Diagram for Buck Converter During Mode I

During this mode, the governing equation is:

$$V_L = V_S - V_O = L\frac{\partial i_L}{\partial t} \qquad (7.1\text{-}2)$$

Solve for

$$i_L(t) = I_1 + \frac{(V_S - V_O)t}{L} \qquad (7.1\text{-}3)$$

Where I_1 is the initial current in inductor L at t=0.

The above equation is valid until the switch S is turned off at $t=t_1$ at which time the inductor current is defined as I_2, the inductor current current at the end of Mode I, where:

$$I_2 = i_L(t_1) = I_1 + \frac{(V_S - V_O)t_1}{L} \qquad (7.1\text{-}4)$$

When switch S is turned off, the inductor current continues to flow through diode D. The interval during which the switch S is turned off is referred to as Mode II. The equivalent circuit for this mode is shown in **Figure 7.4:**

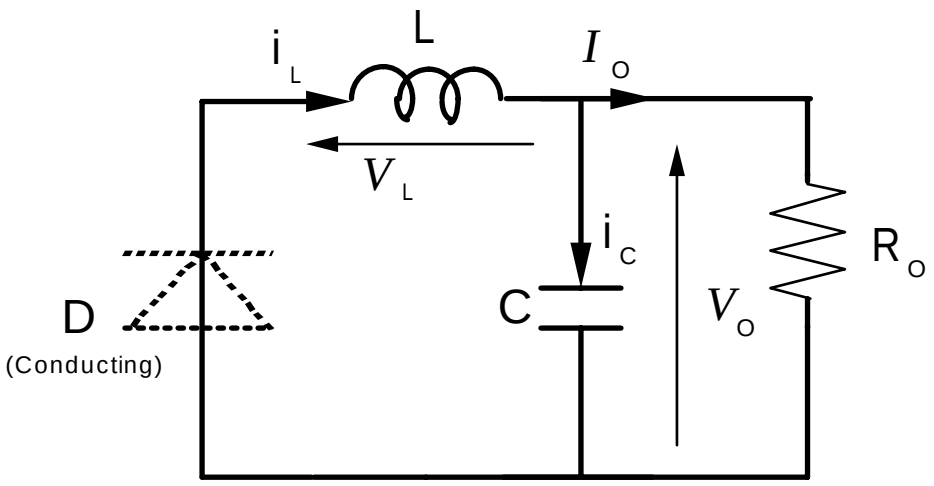


Figure 7.4 Basic Schematic Diagram for Buck Converter During Mode II

During this mode the governing equation is:

$$V_L = -V_O = L\frac{\partial i_L}{\partial t} \qquad (7.1\text{-}5)$$

Solve the above equation for

$$i_L(t) = I_2 - \frac{V_O t}{L} \qquad (7.1\text{-}6)$$

The switch will turn on again at $t=t_2$ at which time the cycle will be back to the same conditions as at t=0 (assuming steady state has been reached). Therefore the inductor current at $t=t_2$ will be same as the initial current, I_1, at t=0 where:

$$I_1 = i_L(t_2) = I_2 - \frac{V_0 t_2}{L} \qquad (7.1\text{-}7)$$

In the steady state I_1 from the end of Mode II will be equal to I_1 from the beginning of Mode I. Similarly, I_2 at the end of Mode I will be equal to I_2 at the beginning of Mode II.

We can obtain two expressions for $I_2 - I_1$:

a) from the end of Mode I;

$$I_2 - I_1 = \frac{(V_S - V_O)t_1}{L} \qquad (7.1\text{-}8)$$

b) from the end of Mode II;

$$I_2 - I_1 = \frac{V_O t_2}{L} \qquad (7.1\text{-}9)$$

Solve the above equations for

$$\frac{V_O t_2}{L} = \frac{(V_S - V_O) t_1}{L} \qquad (7.1\text{-}10)$$

Define the duty cycle, δ ,as;

$$\delta = \frac{t_1}{T} \qquad (7.1\text{-}11)$$

Where $T = t_1 + t_2$ (7.1-12)

$\therefore$ $t_1 = \delta T$ (7.1-13)

and $t_2 = (1-\delta)T$ (7.1-14)

Substitute for t_1 and t_2 into equation (7.1-10) to obtain:

$$V_O(1-\delta) = (V_S - V_O)\delta \qquad (7.1\text{-}15)$$

The above equation can be simplified to;

$$\boxed{V_O = \delta V_S} \qquad (7.1\text{-}16)$$

Also, define the current swing, ΔI, as:

$$\Delta I = I_2 - I_1 = \frac{V_0 t_2}{L} \qquad (7.1\text{-}17)$$

or

$$\boxed{\Delta I = \frac{V_0(1-\delta)}{fL}} \qquad (7.1\text{-}18)$$

where $f = 1/T$ = the switching frequency

Also, if the capacitor C is lossless then the DC current through it will be zero,

and:

$$I_0 = \text{average}(I_L) = (I_1 + I_2)/2 \qquad (7.1\text{-}19)$$

Solve for

$$\boxed{\begin{aligned} I_1 &= I_0 - \frac{\Delta I}{2} \\ I_2 &= I_0 + \frac{\Delta I}{2} \end{aligned}} \qquad (7.1\text{-}20)$$

Also expression for the capacitor current, i_C , can be derived as follows;

$$i_C(t) = i_L(t) - I_0 \qquad (7.1\text{-}21)$$

$$= I_1 - I_0 + \frac{(V_S - V_O)t}{L} \quad \text{during Mode I} \qquad (7.1\text{-}22)$$

$$= -\frac{\Delta I}{2} + \frac{\Delta I t}{t_1} \qquad (7.1\text{-}23)$$

and $$i_C(t) = \frac{\Delta I}{2} - \frac{\Delta I t}{t_2} \quad \text{during Mode II} \qquad (7.1\text{-}24)$$

Therefore the peak to peak ripple current in the capacitor can be determined from the above equations:

$$\boxed{\Delta I_C = \frac{V_0(1-\delta)}{fL}} \qquad (7.1\text{-}25)$$

Also the peak to peak ripple voltage in ΔV_0 can be determined by integrating the ripple current in the output capacitor;

$$\Delta V_0 = \Delta V_C = \frac{1}{C}\int_{\frac{t_1}{2}}^{t_1} i_c(t)\partial t + \frac{1}{C}\int_0^{\frac{t_2}{2}} i_c(t)\partial t \qquad (7.1\text{-}26)$$

$$= \frac{1}{C}\int_{\frac{t_1}{2}}^{t_1}\left[\frac{\Delta I}{2} - \frac{\Delta I t}{t_1}\right]\partial t + \frac{1}{C}\int_{0}^{\frac{t_2}{2}}\left[\frac{\Delta I}{2} - \frac{\Delta I t}{t_2}\right]\partial t \qquad (7.1\text{-}27)$$

$$= \frac{\Delta I}{2C}\left[-t + \frac{t^2}{t_1}\right]_{\frac{t_1}{2}}^{t_1} + \frac{\Delta I}{2C}\left[t - \frac{t^2}{t_2}\right]_{0}^{\frac{t_2}{2}} \qquad (7.1\text{-}28)$$

$$= \frac{\Delta I}{2C}\left[\frac{t_1}{4}\right] + \frac{\Delta I}{2C}\left[\frac{t_2}{4}\right] \qquad (7.1\text{-}29)$$

$$= \frac{\Delta I}{8C}(t_1 + t_2) \qquad (7.1\text{-}30)$$

$$\therefore \quad \Delta V_C = \frac{\Delta I}{8C} T = \frac{\Delta I}{8fC} \quad \text{peak to peak} \qquad (7.1\text{-}31)$$

Also one can substitute for $\Delta I = \frac{V_0(1-\delta)}{fL}$ to obtain;

$$\boxed{\Delta V_C = \frac{V_0(1-\delta)}{8f^2LC}} \quad (7.1\text{-}32)$$

Note the above expression for peak to peak ripple does not include "switching spikes" which appear on the output due to high frequency components of the switching waveform which get through the L and C of the output filter.

In particular, the major component of ripple is often due to the equivalent series resistance, E_{SR} , in the output capacitor combined with the ripple current in this capacitor. This component of output ripple is referred to as ΔV_R , where;

$$\Delta V_R = \Delta I_C E_{SR} \quad \text{peak to peak} \qquad (7.1\text{-}33)$$

Usually one of the above, ΔV_C or ΔV_R , dominates. At high frequencies it's ΔV_R , at low frequencies it's ΔV_C .

Note that in the entire preceding analysis it was assumed that the inductor current, i_L , never went to zero.

i.e. $I_1 > 0$ (7.1-34)

Substitute for $I_1 = I_0 - \frac{V_0(1-\delta)}{2fL} > 0$ (7.1-35)

and solve for

$$L > \frac{V_0(1-\delta)}{2fI_0} \quad (7.1\text{-}36)$$

This is defined as the critical inductance, L_C , where;

$$\boxed{L_C = \frac{V_0(1-\delta)}{2fI_0}} \quad (7.1\text{-}37)$$

This gives us the critical, minimum, value for L that will maintain the above equations for ΔI, ΔV_C , I_1 , I_2 and V_O .

Conversely, for any given value of L we can solve for the critical, minimum, value of I_0 ;

$$\boxed{I_{min.} > \frac{V_0(1-\delta)}{2fL}} \quad (7.1\text{-}38)$$

This gives us the critical, minimum, value for load on the Buck Converter, I_0 , that will maintain the above equations for ΔI, ΔV_C , I_1 , I_2 and V_O .

Also, for resistive loads;

$$I_O = \frac{V_O}{R_O} = \frac{\delta V_S}{R_O} \quad (7.1\text{-}39)$$

And the output power P_O , can be determined;

$$P_O = I_O V_O = \frac{\delta^2 V_S^2}{R_O} \quad (7.1\text{-}40)$$

For an ideal (lossless) Buck Converter, the input power will be equal to the output power;

$$P_{in} = P_O \quad (7.1\text{-}41)$$

or;

$$I_{in} V_S = \frac{\delta^2 V_S^2}{R_O} \quad (7.1\text{-}42)$$

Solve for;

$$I_{in} = \frac{\delta^2 V_S}{R_O} = \delta I_O \quad (7.1\text{-}43)$$

Also the bulk input impedance, R_{in} , can be determined, where;

$$R_{in} = V_S / I_{in} = \frac{R_O}{\delta^2} \quad (7.1\text{-}44)$$

Therefore a buck converter acts like a DC to DC transformer with a turns ratio of δ.

Example Problem 7-1

Design a Buck Converter to meet the following requirements:

V_S = 300 Vdc ± 50 Vdc

V_O = 50 Vdc

Maximum ripple = 200 mV peak to peak

I_O = 1 Amp minimimum, 25 A maximum

Switching frequency is 200 kHz

Determine:

a) The duty cycle, δ, at minimum, nominal and maximum input voltage.

b) The critical inductance required and average and peak current rating for the inductor.

c) The peak to peak ripple current in the output capacitor.

d) The output capacitance required, assuming zero E_{SR} .

e) The output capacitance required assuming an E_{SR} of 0.8 Ω per 1000μF can.

f) The peak voltage and current for the diode and transistor switch.

Solution:

a) $V_O = \delta V_S$ therefore $\delta = \frac{V_O}{V_S}$

at minimum V_S δ = 50/(300 - 50) = 0.2

at nominal V_S δ = 50/300 = 0.167

at maximum V_S δ = 50/(300 + 50) = 0.143

b) $L_C = \frac{V_0(1-\delta)}{2fI_0}$ for worst case δ = minimum and I_O = minimum

Therefore:

$L_C = \frac{50\times(1-0.143)}{2\times200\times10^3\times1}$ = 107 μH

$\bar{I} = I_O$ = 25 A worst case

$\hat{I} = I_2 = I_0 + \frac{\Delta I}{2}$

and $\Delta I = \frac{V_0(1-\delta)}{fL_C} = \frac{50\times(1-0.143)}{200\times10^3\times107\times10^{-6}}$ = 2 A

Substitute into the expression for to obtain:

$\hat{I} = I_0 + \frac{\Delta I}{2} = 25 + \frac{2}{2} = 26$ A

c) $\Delta I_C = \Delta I$ = 2.0 A

d) $\Delta V_C = \frac{V_0(1-\delta)}{8f^2LC}$

Solve for C = $\frac{V(1-\delta)}{8f^2L\Delta V_c} = \frac{50\times(1-0.143)}{8\times\left[200\times10^3\right]^2\times107\times10^{-6}\times0.2}$

= 6.25 μF

e) $\Delta V_R = \Delta I_C E_{SR}^{Total}$

Solve for:

$E_{SR}^{Total} = \frac{\Delta V_R}{\Delta I_C}$

Where E_{SR}^{Total} represents the total equivalent E_{SR} of all the capacitors in the output filter. Typically this consists of a number of capacitor "cans" connected in parallel, and thus:

$E_{SR}^{Total} = \frac{E_{SR}}{N_C}$ Where N_C represents the number of cans

Therefore solve for:

$N_C = \frac{E_{SR}}{E_{SR}^{Total}} = \frac{E_{SR}\,\Delta I_C}{\Delta V_R} = \frac{0.8\times2}{0.2} = 8$

Total capacitance $C^{Total} = N_C\,C^C$ where C^C is the capacitance per can

Therefore $C^{Total} = 8\times1000 = 8000$ μF

f) Peak voltage for diode and transistor is:

$\hat{V}_D = \hat{V}_Q = V_S$ = 300 + 50 = 350 V worst case

Peak current for diode and transistor is:

$\hat{I}_D = \hat{I}_Q = I_2$ = 26 A worst case

7.2 BOOST CONVERTER (also known as a Boost Regulator)

The basic schematic circuit diagram for a Boost Converter is shown in **Figure 7.5**.

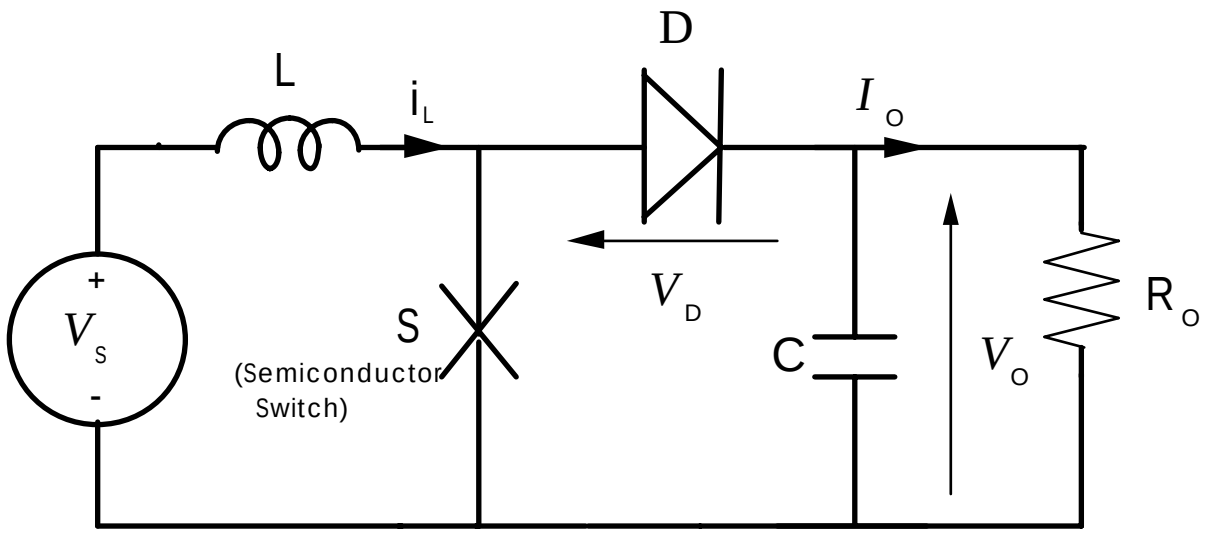


FIGURE 7.5 Basic Schematic Diagram For a Boost Converter

Switch S is turned on for t_1 seconds and then turned off for t_2 seconds such that:

$$t_1 + t_2 = T \qquad (7.2\text{-}1)$$

where T is the period for one switching cycle.

We can assume that the output capacitor C is large enough such that V_o is constant and therefore I_o is also constant during the switching period.

When the switch S is turned on at $t=0$, diode D becomes reverse biased and acts as an open circuit. This is referred to a Mode I and the equivalent circuit for this mode is shown in **Figure 7.6**

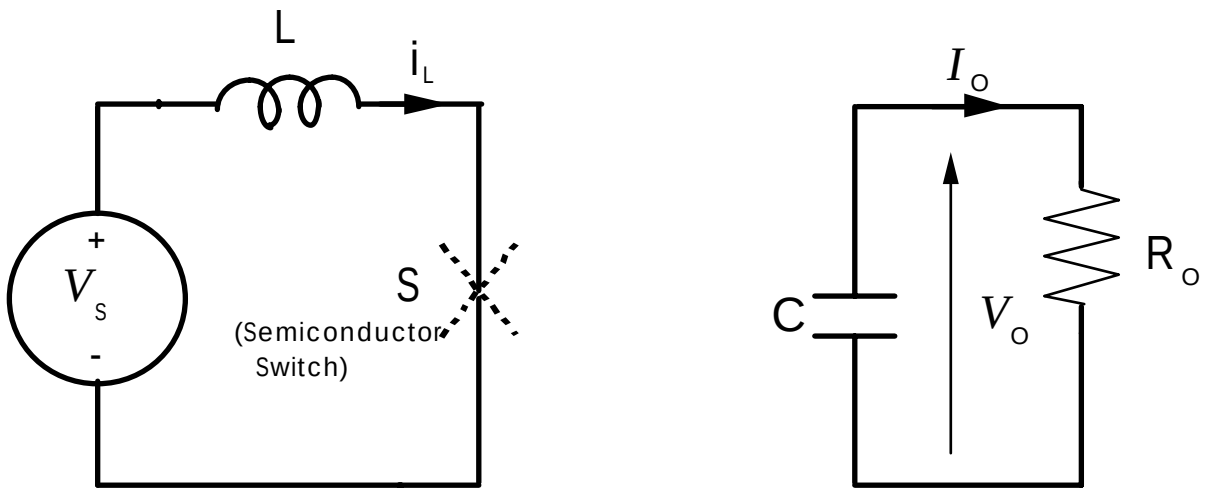


FIGURE 7.6 Equivalent Circuit During Mode I

During this mode, the governing equation is:

$$V_L = V_S = L\frac{\partial i_L}{\partial t} \qquad (7.2\text{-}2)$$

Solve for

$$i_L(t) = I_1 + \frac{V_S t}{L} \qquad (7.2\text{-}3)$$

Where I_1 is the initial current in inductor L at t=0.

The above equation is valid until the switch S is turned off at $t=t_1$ at which time the inductor current is defined as I_2 , the inductor current at the end of Mode I, where:

$$I_2 = i_L(t_1) = I_1 + \frac{V_S t_1}{L} \qquad (7.2\text{-}4)$$

When switch S is turned off, the inductor current continues to flow through diode D. The interval during which the switch S is turned off is referred to as Mode II. The equivalent circuit for this mode is shown in **Figure 7.7**:

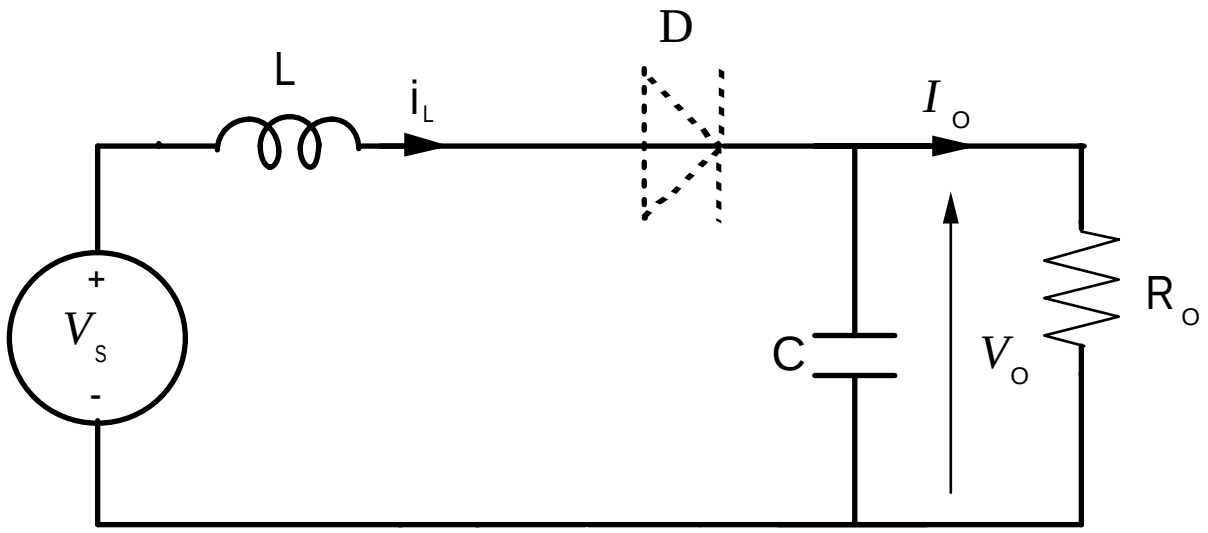


Figure 7.7 Equivalent Circuit During Mode II

During this mode the governing equation is:

$$V_L = V_S - V_O = L\frac{\partial i_L}{\partial t} \qquad (7.2\text{-}5)$$

Solve for;

$$i_L(t) = I_2 + \frac{(V_S - V_O)t}{L} \qquad (7.2\text{-}6)$$

The above equations are valid until the switch turns on again at $t=t_2$, at which time the inductor current will be I_1 again, assuming steady state conditions, where;

$$I_1 = i_L(t_2) = I_2 + \frac{(V_S - V_O)t_2}{L} \qquad (7.2\text{-}7)$$

We can obtain two expressions for $I_2 - I_1$:

a) from the end of Mode I, equation (7.2-4) can be rewritten as;

$$I_2 - I_1 = \frac{V_S t_1}{L} \qquad (7.2\text{-}8)$$

b) from the end of Mode II, equation (7.2-7) can be rewritten as;

$$I_2 - I_1 = \frac{(V_O - V_S)t_2}{L} \qquad (7.2\text{-}9)$$

Solve the above equations for

$$\frac{V_S t_1}{L} = \frac{(V_O - V_S)t_2}{L} \qquad (7.2\text{-}10)$$

Define the duty cycle, δ ,as;

$$\delta = \frac{t_1}{T} \qquad (7.2\text{-}11)$$

Where $T = t_1 + t_2$ (7.2-12)

$\therefore$ $t_1 = \delta T$ (7.2-13)

and $t_2 = (1-\delta)T$ (7.2-14)

Substitute for t_1 and t_2 into equation (7.2-11) to obtain: (7.2-15)

$$V_S \delta = (V_O - V_S)(1-\delta) \qquad (7.2\text{-}16)$$

The preceeding equation can be simplified to;

$$V_O = \frac{V_S(t_1 + t_2)}{t_2} = \frac{V_S}{(1-\delta)} \qquad (7.2\text{-}17)$$

or

$$\boxed{V_O = \frac{V_S}{(1 - \delta)}} \qquad (7.2\text{-}18)$$

Note, that δ is always less than 1, and therefore V_O will always be greater than V_S , i.e. the output voltage is "boosted" above the input voltage.

Also, define the current swing, ΔI, as:

$$\Delta I = I_2 - I_1 = \frac{V_S t_1}{L} \qquad (7.2\text{-}19)$$

or

$$\boxed{\Delta I = \frac{V_0 \delta(1-\delta)}{fL}} \qquad (7.2\text{-}20)$$

where $f = 1/T$ = the switching frequency (7.2-21)

Also, if the capacitor C is lossless then the DC current through it will be zero, and:

$$I_0 = \text{average}\,(I_D) = (I_1 + I_2)(1-\delta)/2 \qquad (7.2\text{-}22)$$

Solve for

$$\boxed{\begin{aligned} I_1 &= \frac{I_0}{1-\delta} - \frac{\Delta I}{2} \\ I_2 &= \frac{I_0}{1-\delta} + \frac{\Delta I}{2} \end{aligned}} \qquad (7.2\text{-}23)$$

Also the capacitor current, i_C , can be derived as follows;

$$i_C(t) = -I_0 \quad \text{during Mode I} \qquad (7.2\text{-}24)$$

and $$i_C(t) = i_L(t) - I_0 \quad \text{during Mode II} \qquad (7.2\text{-}25)$$

$$= I_2 + \frac{(V_S - V_O)t}{L} - I_0 \qquad (7.2\text{-}26)$$

Therefore the peak to peak ripple current in the capacitor can be determined from the above equations:

$$\Delta I_C = I_2 \qquad (7.2\text{-}27)$$

or

$$\boxed{\Delta I_C = \frac{I_0}{1-\delta} + \frac{\Delta I}{2}} \qquad (7.2\text{-}28)$$

Also the peak to peak ripple voltage, ΔV_C , can be determined by integrating the ripple current in the output capacitor;

$$\Delta V_C = \frac{1}{C}\int_0^{t_1} i_c(t)\partial t \qquad (7.2\text{-}29)$$

$$= \frac{1}{C}\int_0^{t_1} I_o \partial t \qquad (7.2\text{-}30)$$

$$\therefore \quad \Delta V_C = \frac{I_0 t_1}{C} = \frac{I_0 \delta}{fC} \quad \text{peak to peak} \qquad (7.2\text{-}31)$$

Note the above expression for peak to peak ripple does not include "switching spikes" which appear on the output due to high frequency components of the switching waveform which get through the L and C of the output filter.

In particular, the major component of ripple is often due to the equivalent series resistance, E_{SR} , in the output capacitor combined with the ripple current in this capacitor. This component of output ripple is referred to as ΔV_R , where;

$$\Delta V_R = \Delta I_C E_{SR} \quad \text{peak to peak} \qquad (7.2\text{-}32)$$

or

$$\boxed{\Delta V_R = \left[\frac{I_0}{1-\delta} + \frac{\Delta I}{2}\right] E_{SR}} \qquad (7.2\text{-}33)$$

Usually one of the above, ΔV_C or ΔV_R , dominates. At high frequencies it's ΔV_R , at low frequencies it's ΔV_C .

Note that in the entire preceeding analysis it was assumed that the inductor current, i_L , never went to zero.

i.e. $I_1 > 0 \qquad (7.2\text{-}34)$

Substitute for $I_1 = \frac{I_0}{1-\delta} - \frac{\Delta I}{2} > 0 \qquad (7.2\text{-}35)$

or

$$I_1 = \frac{I_0}{1-\delta} - \frac{V_0 \delta(1-\delta)}{2fL} > 0 \qquad (7.2\text{-}36)$$

and solve for;

$$L > \frac{V_0\delta(1-\delta)^2}{2fI_0} \qquad (7.2\text{-}37)$$

This is defined as the critical inductance, L_C , where;

$$\boxed{L_C = \frac{V_0\delta(1-\delta)^2}{2fI_0}} \qquad (7.2\text{-}38)$$

This gives us the critical, minimum, value for L that will maintain the above equations for ΔI, ΔV_C , I_1 , I_2 and V_O .

Conversely, for any given value of L we can solve for the critical, minimum, value of I_0 ;

$$\boxed{I_{min.} > \frac{V_0\delta(1-\delta)^2}{2fL}} \qquad (7.2\text{-}39)$$

This gives us the critical, minimum, value for load on the Buck Converter, I_0 , that will maintain the above equations for ΔI, ΔV_C , I_1 , I_2 and V_O .

Also, for resistive loads;

$$I_O = \frac{V_O}{R_O} = \frac{V_S}{R_O(1-\delta)} \qquad (7.2\text{-}40)$$

And the output power P_O , can be determined;

$$P_O = I_O V_O = \frac{V_S^2}{R_O(1-\delta)^2} \qquad (7.2\text{-}41)$$

For an ideal (lossless) Boost Converter, the input power will be equal to the output power;

$$P_{in} = P_O \qquad (7.2\text{-}42)$$

or;

$$I_{in} V_S = \frac{V_S^2}{R_O(1-\delta)^2} \qquad (7.2\text{-}43)$$

Solve for;

$$I_{in} = \frac{V_S}{R_O(1-\delta)^2} = \frac{I_O}{(1-\delta)} \qquad (7.2\text{-}44)$$

Also the input impedance, R_{in} , can be determined;

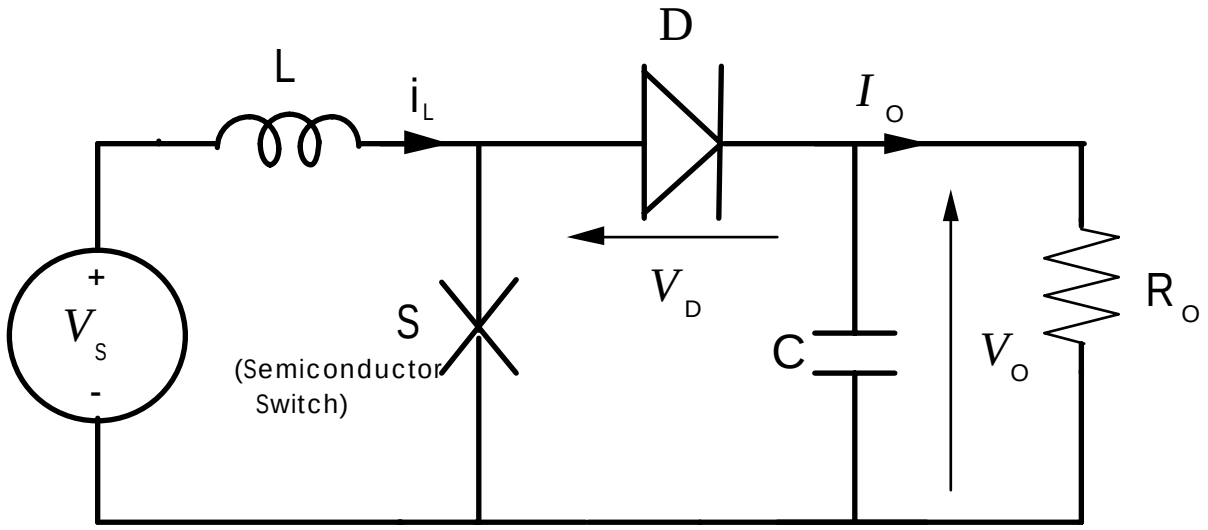
$$R_{in} = V_S / I_{in} = R_O(1 - \delta)^2 \qquad (7.2\text{-}45)$$

Therefore a boost converter acts like a DC to DC transformer with a turns ratio of $(1-\delta)$.

Example Problem 7-2

You are given a 50 µF capacitor with E_{SR} = 100 mΩ and a 25 µH inductor.
Design a **Boost Converter** using these components to meet the following:
V_s =36 Vdc minimum, 72 Vdc maximum
V_o = 150 Vdc, 1% peak to peak ripple, I_o = 0.1 A minimum, 2.0 A maximum
Draw the equivalent circuit and determine:
a) The minimum and maximum δ.
b) The minimum switching frequency that will keep the inductor current from going to zero.
c) The minimum switching frequency to meet the output ripple requirement.
d) The minimum switching frequency to meet both b) and c) above.
e) The variation in output voltage (in ±%) if the input voltage is 50 V and the transistor "on time" varies by ±1%.

Solution:



Equivalent Circuit
a) Min and Max δ:

$$V_O = \frac{V_S}{(1 - \delta)}$$

Solve for

$$\delta = 1 - \frac{V_S}{V_O} = 1 - \frac{72}{150} = 0.52 \text{ min.}$$

$$= 1 - \frac{36}{150} = 0.76 \text{ max.}$$

b) minimum frequency to keep inductor current from going to zero:

$$I_{min.} = \frac{V_0 \delta (1-\delta)^2}{2fL}$$

Solve for:

$$f = \frac{V_0\delta(1-\delta)^2}{2LI_{min.}} = \frac{150 \times 0.52 \times (1-0.52)^2}{2 \times 25\times10^{-6} \times 0.1} = 3.59 \text{ MHz}$$

c) minimum frequency to meet ripple voltage:

$$\Delta V_C = \frac{I_0\delta}{fC}$$

Solve for:

$$f = \frac{I_0\delta}{C\Delta V_C} = \frac{2 \times 0.76}{50 \times 150 \times 1\%} = 20.2 \text{ kHz}$$

Also:

$$\Delta V_R = \left[\frac{I_0}{1-\delta} + \frac{\Delta I}{2}\right] E_{SR}$$

Solve for:

$$\left[\frac{I_0}{1-\delta} + \frac{\Delta I}{2}\right] = \frac{\Delta V_R}{E_{SR}} = \frac{150 \times 1\%}{0.1} = 15 \text{ A}$$

Rearrange to solve for:

$$\Delta I = 2\left[\frac{\Delta V_R}{E_{SR}} - \frac{I_0}{1-\delta}\right]$$

And:

$$\Delta I = \frac{V_0\delta(1-\delta)}{fL}$$

Solve for f then substitute for ΔI to obtain:

$$f = \frac{V_0\delta(1-\delta)}{L\Delta I} = \frac{V_0\delta(1-\delta)}{2L\left[\frac{\Delta V_R}{E_{SR}} - \frac{I_0}{1-\delta}\right]}$$

$$= \frac{150 \times 0.52 \times (1-0.52)}{2 \times 25\times10^{-6} \times \left[15 - \frac{2}{1-0.52}\right]} = 69.1 \text{ KHz} \quad \text{at } \delta = 0.52$$

$$= \frac{150 \times 0.76 \times (1-0.76)}{2 \times 25\times10^{-6} \times \left[15 - \frac{2}{1-0.76}\right]} = 82.1 \text{ KHz} \quad \text{at } \delta = 0.76$$

Therefore frequency must be at least 82.1 KHz to meet both ΔV_R and ΔV_C

d) Overall minimum frequency is therefore the higher answer from b) and c):

f = 3.59 MHz

e) The variation in output voltage (in ±%) if the input voltage is 50 V and the transistor "on time" varies by ±1%.
At 50V input:

$$\delta = 1 - \frac{V_S}{V_O} = 1 - \frac{50}{150} = 0.667$$

and

$$V_O = \frac{V_S}{(1 - \delta)} = \frac{50}{(1 - 0.667 \times 1.01)} = 153.06 \text{ V} = 150 + 2.05\%$$

$$= \frac{50}{(1 - 0.667 \times 0.99)} = 147.06 \text{ V} = 150 - 1.96\%$$

$$\approx 150 \text{ V} \pm 2\%$$

7.3 BUCK-BOOST CONVERTER (also known as a Buck-Boost Regulator)

The basic schematic circuit diagram for a Buck-Boost Converter is shown in **Figure 7.8**.

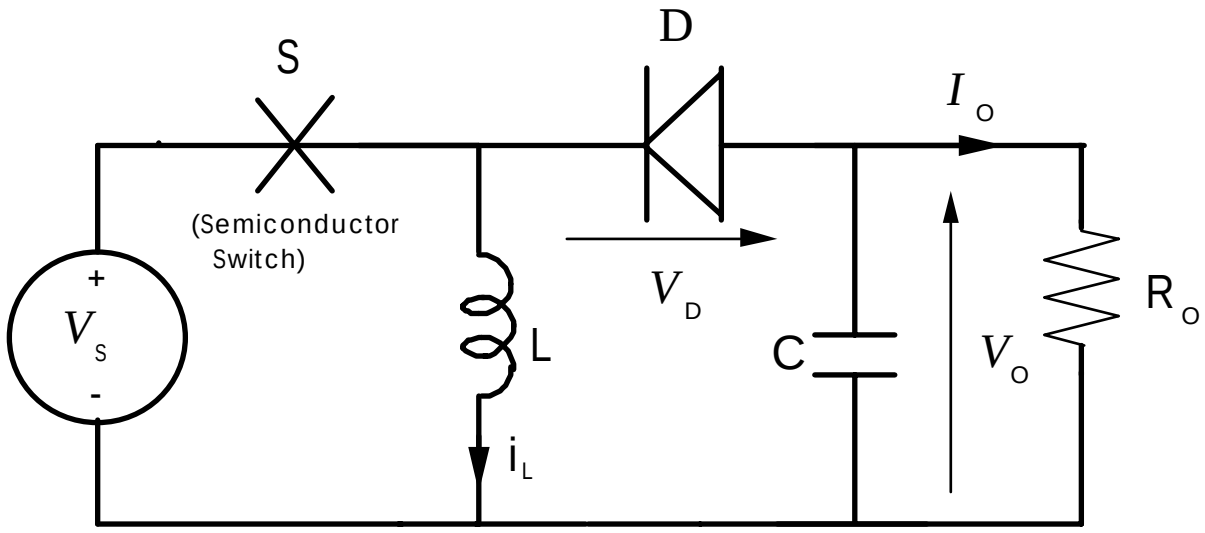


Figure 7.8 Basic Schematic Diagram For a Buck-Boost Converter

Switch S is turned on for t_1 seconds and then turned off for t_2 seconds such that:

$$t_1 + t_2 = T \qquad (7.3\text{-}1)$$

where T is the period for one switching cycle.

We can assume that the output capacitor C is large enough such that V_o is constant and therefore I_o is also constant during the switching period.

When the switch S is turned on at t=0, diode D becomes reverse biased and acts as an open circuit. This is referred to as Mode I and the equivalent circuit for this mode is shown in **Figure 7.9.**

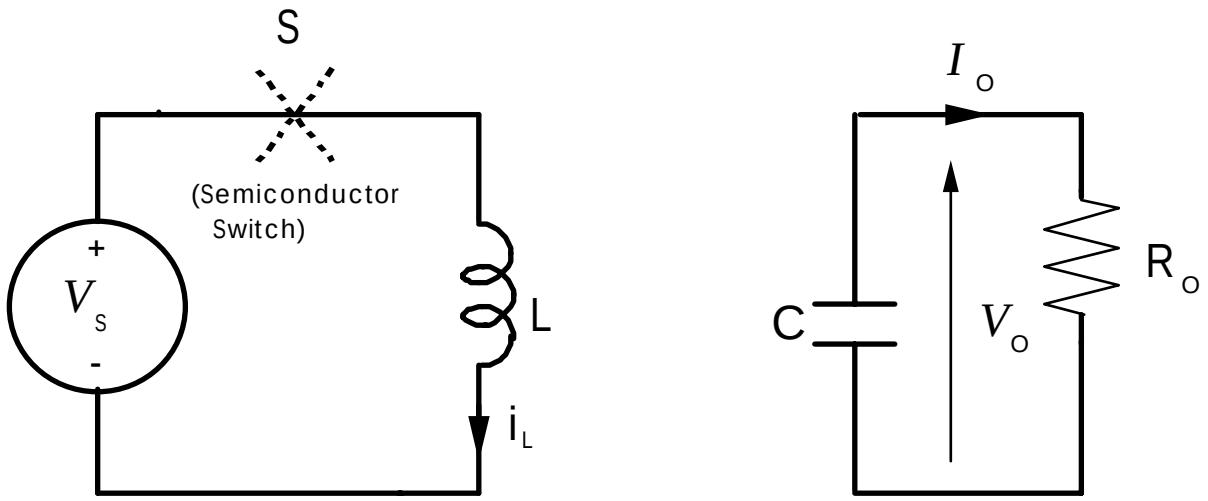


Figure 7.9 Equivalent Circuit During Mode I

During this mode, the governing equation is:

$$V_L = V_S = L\frac{\partial i_L}{\partial t} \qquad (7.3\text{-}2)$$

Solve for

$$i_L(t) = I_1 + \frac{V_S t}{L} \qquad (7.3\text{-}3)$$

Where I_1 is the initial current in inductor L at t=0.

The above equation is valid until the switch S is turned off at $t=t_1$ at which time the inductor current is defined as I_2 , the inductor current at the end of Mode I, where:

$$I_2 = i_L(t_1) = I_1 + \frac{V_S t_1}{L} \qquad (7.3\text{-}4)$$

When switch S is turned off, the inductor current continues to flow through the parallel combination of C and R_O, and back through diode D. The equivalent circuit for this mode is shown in **Figure 7.10**:

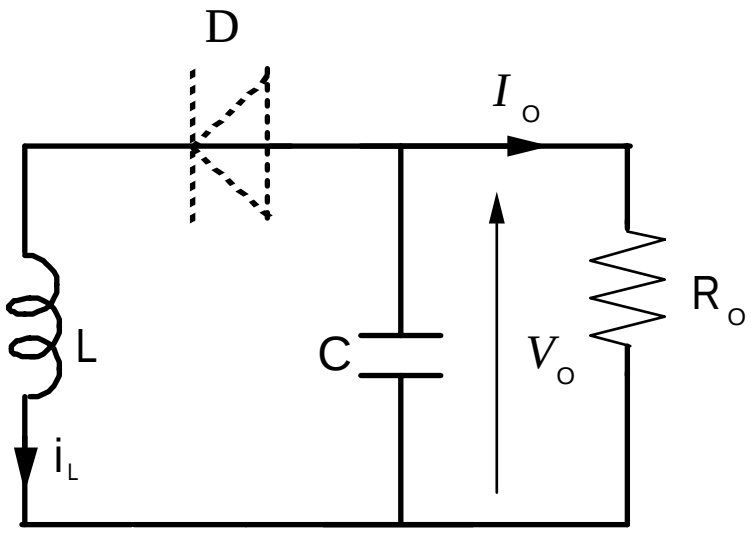


Figure 7.10 Equivalent Circuit During Mode II

During this mode the governing equation is:

$$V_L = V_O = L\frac{\partial i_L}{\partial t} \tag{7.3-5}$$

Solve for;

$$i_L(t) = I_2 + \frac{V_O t}{L} \tag{7.3-6}$$

The above equations are valid until the switch turns on again at $t=t_2$, at which time the inductor current will be I_1 again, assuming steady state conditions, where;

$$I_1 = i_L(t_2) = I_2 + \frac{V_O t_2}{L} \tag{7.3-7}$$

We can obtain two expressions for $I_2 - I_1$:

a) from the end of Mode I, equation (7.3-4) can be rewritten as;

$$I_2 - I_1 = \frac{V_S t_1}{L} \tag{7.3-8}$$

b) from the end of Mode II, equation (7.3-7) can be rewritten as;

$$I_2 - I_1 = -\frac{V_O t_2}{L} \qquad (7.3\text{-}9)$$

Solve the above equations for

$$\frac{V_S t_1}{L} = -\frac{V_O t_2}{L} \qquad (7.3\text{-}10)$$

Define the duty cycle, δ ,as;

$$\delta = \frac{t_1}{T} \qquad (7.3\text{-}11)$$

Where $T = t_1 + t_2$ (7.3-12)

$\therefore$ $t_1 = \delta T$ (7.3-13)

and $t_2 = (1-\delta)T$ (7.3-14)

Substitute for t_1 and t_2 into equation (7.3-10) to obtain:

$$V_S \delta = -V_O(1-\delta) \qquad (7.3\text{-}15)$$

The above equation can be simplified to;

$$\boxed{V_O = \frac{-\delta V_S}{(1-\delta)}} \qquad (7.3\text{-}16)$$

Note that the Buck-Boost is an <u>inverting</u> converter, the output voltage is inverse polarity with respect to the input voltage, and;

$|V_o| < |V_s|$ for $\delta < 0.5$ (7.3-17)

$|V_o| > |V_s|$ for $\delta > 0.5$ (7.3-18)

Also, define the current swing, ΔI, as:

$$\Delta I = I_2 - I_1 = \frac{V_S t_1}{L} \qquad (7.3\text{-}19)$$

or

$$\Delta I = \frac{V_0(1-\delta)}{fL} \qquad (7.3\text{-}20)$$

where $f = 1/T$ = the switching frequency (7.3-21)

Also, if the capacitor, C, is lossless then the DC current through it will be zero, and:

$$I_0 = -\text{ average } (I_D) = (I_1 + I_2)(\delta - 1)/2 \qquad (7.3\text{-}22)$$

Solve for

$$I_1 = \frac{I_0}{1-\delta} - \frac{\Delta I}{2}$$
$$I_2 = \frac{I_0}{1-\delta} + \frac{\Delta I}{2} \qquad (7.3\text{-}23)$$

Also the capacitor current, i_C , can be derived as follows;

$$i_C(t) = -I_0 \quad \text{during Mode I} \qquad (7.3\text{-}24)$$

and $$i_C(t) = -i_L(t) - I_0 \quad \text{during Mode II} \qquad (7.3\text{-}25)$$

$$= -I_2 - \frac{V_O t}{L} - I_0 \qquad (7.3\text{-}26)$$

Therefore the peak to peak ripple current in the capacitor can be determined from the above equations:

$$\Delta I_C = I_2 \qquad (7.3\text{-}27)$$

or

$$\Delta I_C = \frac{I_0}{1-\delta} + \frac{\Delta I}{2} \qquad (7.3\text{-}28)$$

Also the peak to peak ripple voltage, ΔV_C , can be determined by integrating the ripple current in the output capacitor;

$$\Delta V_C = \frac{1}{C}\int_0^{t_1} i_c(t)\partial t \qquad (7.3\text{-}29)$$

$$= \frac{1}{C}\int_0^{t_1} I_o \partial t \qquad (7.3\text{-}30)$$

$$\therefore \quad \Delta V_C = \frac{I_0 t_1}{C} = \frac{I_0 \delta}{fC} \quad \text{peak to peak} \qquad (7.3\text{-}31)$$

Note the above expression for peak to peak ripple does not include "switching spikes" which appear on the output due to high frequency components of the switching waveform which get through the L and C of the output filter.

In particular, the major component of ripple is often due to the equivalent series resistance, E_{SR} , in the output capacitor combined with the ripple current in this capacitor. This component of output ripple is referred to as ΔV_R , where;

$$\Delta V_R = \Delta I_C E_{SR} \quad \text{peak to peak} \qquad (7.3\text{-}32)$$

or

$$\boxed{\Delta V_R = \left[\frac{I_0}{1-\delta} + \frac{\Delta I}{2}\right] E_{SR}} \qquad (7.3\text{-}33)$$

Usually one of the above, ΔV_C or ΔV_R , dominates. At high frequencies it's ΔV_R , at low frequencies it's ΔV_C .

Note that in the entire preceding analysis it was assumed that the inductor current, i_L , never went to zero.

i.e. $I_1 > 0 \qquad (7.3\text{-}34)$

Substitute for $I_1 = \frac{I_0}{1-\delta} - \frac{\Delta I}{2} > 0 \qquad (7.3\text{-}35)$

or

$$I_1 = \frac{I_0}{1-\delta} - \frac{V_0(1-\delta)}{2fL} > 0 \qquad (7.3\text{-}36)$$

and solve for;

$$L > \frac{V_0(1-\delta)^2}{2fI_0} \qquad (7.3\text{-}37)$$

This is defined as the critical inductance, L_C , where;

$$\boxed{L_C = \frac{V_0(1-\delta)^2}{2fI_0}} \qquad (7.3\text{-}38)$$

This gives us the critical, minimum, value for L that will maintain the above equations for ΔI, ΔV_C , I_1 , I_2 and V_O .

Conversely, for any given value of L we can solve for the critical, minimum, value of I_0 ;

$$\boxed{I_{min.} > \frac{V_0(1-\delta)^2}{2fL}} \qquad (7.3\text{-}39)$$

This gives us the critical, minimum, value for load on the Buck Converter, I_0 , that will maintain the above equations for ΔI, ΔV_C , I_1 , I_2 and V_O .

Also, for resistive loads;

$$I_O = \frac{V_O}{R_O} = \frac{-\delta V_S}{R_O(1-\delta)} \qquad (7.3\text{-}40)$$

And the output power P_O , can be determined;

$$P_O = I_O V_O = \frac{\delta^2 V_S^2}{R_O(1-\delta)^2} \qquad (7.3\text{-}41)$$

For an ideal (lossless) Boost Converter, the input power will be equal to the output power;

$$P_{in} = P_O \qquad (7.3\text{-}42)$$

or;

$$I_{in} V_S = \frac{\delta^2 V_S^2}{R_O(1-\delta)^2} \qquad (7.3\text{-}43)$$

Solve for;

$$I_{in} = \frac{\delta^2 V_S}{R_O(1-\delta)^2} = -\frac{\delta I_O}{(1-\delta)} \qquad (7.3\text{-}44)$$

Also the input impedance, R_{in} , can be determined;

$$R_{in} = V_S / I_{in} = R_O(1-\delta)^2 / \delta^2 \qquad (7.3\text{-}45)$$

Therefore a boost converter acts like a DC to DC transformer with a

turns ratio of $(1 - \delta)/\delta$

.

Example Problem 7-3:
Design a **BUCK-BOOST converter** to meet the following requirements:

Input Voltage, V_{in} = 320 ± 80 Vdc

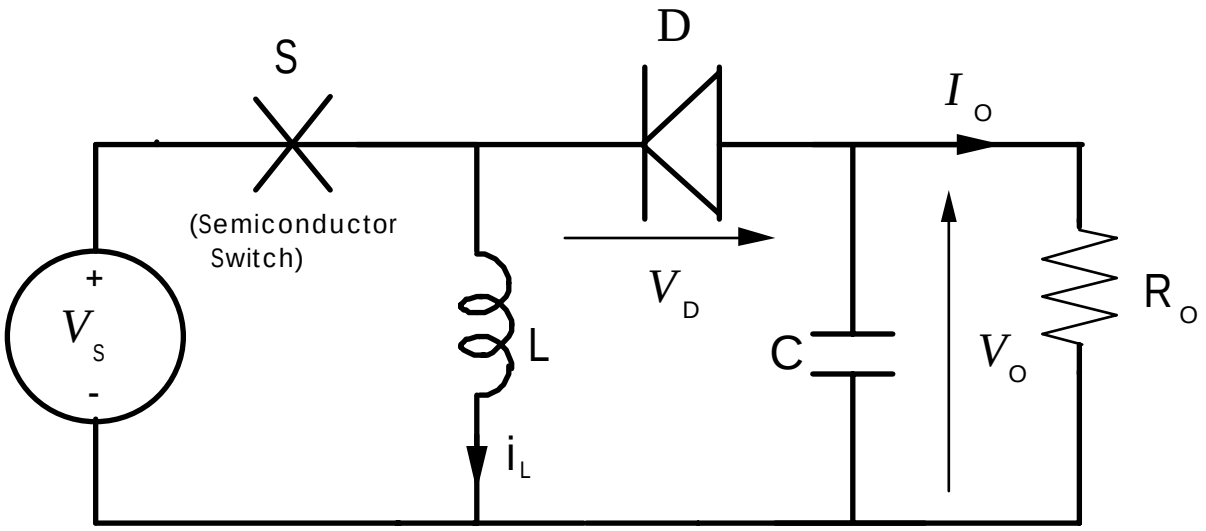
Output Voltage, V_o = -3.3Vdc with a maximum ripple of 30mV p-p.

Output Current, I_o = 0.5 A minimum, 2.0 A maximum.

Switching frequency f = 125 kHz

Determine the following:
a) The duty cycle at minimum and maximum input voltage
b) The critical inductance.
c) The minimum number of output capacitors if each capacitor has 1,000 µF and an E_{sr} of 10 mΩ.
d) The peak current and voltage ratings for the semiconductors.
e) The variation in output voltage at nominal input and if the transistor on time varies by ± 0.008µs:

Solution:



Basic circuit diagram for a buck-boost converter

a) Duty cycle at min and max input voltage:

$$V_O = \frac{-\delta V_S}{(1-\delta)}$$

Solve for:

$$\delta = \frac{V_O}{V_O - V_S} = \frac{-3.3}{-3.3 - 240} = 0.0136 \text{ @ minimum } V_S$$

$$= \frac{-3.3}{-3.3 - 400} = 0.00818 \text{ @ maximum } V_S$$

c) The critical inductance:

$$L_C = \frac{V_O(1-\delta)^2}{2fI_O} = \frac{3.3 \times (1 - 0.00818)^2}{2 \times 125\times10^3 \times 0.5} = 26.0\ \mu H$$

d) The minimum number of output capacitors if each capacitor has 1,000 µF and an E_{sr} of 10 mΩ:

$$\Delta V_C = \frac{I_O\delta}{fC}$$

Solve for:

$$C = \frac{I_O\delta}{f\Delta V_C} = \frac{2 \times 0.0136}{125\times10^3 \times 30\times10^{-3}} = 7.25\ \mu F$$

Therefore one 1,000 µF capacitor would be required if ΔV_C were the determining criteria.

Also:

$$\Delta V_R = \left[\frac{I_0}{1-\delta} + \frac{\Delta I}{2}\right] E_{SR}$$

Where:

$$\Delta I = \frac{V_O(1-\delta)}{fL_m}$$

Substitute for ΔI to obtain:

$$E_{SR} = \frac{\Delta V_R}{\left[\frac{I_0}{1-\delta} + \frac{\Delta I}{2}\right]}$$

$$= \frac{\Delta V_R}{\left[\frac{I_0}{1-\delta} + \frac{V_O(1-\delta)}{2fL_m}\right]} = \frac{30\times10^{-3}}{\left[\frac{2}{1 - 0.0136} + \frac{3.3\times10^{-3}}{2 \times 125\times10^3 \times 26.0\times10^{-6}}\right]}$$

$$= 11.9\ m\Omega$$

Therefore one 1,000 µF capacitor would be required if ΔV_R were the determining criteria.

Therefore the correct number of capacitors is 1.

e) The peak current and voltage ratings for the semiconductors:

$$\hat{I}_Q = \hat{I}_D = \frac{I_0}{1-\delta} + \frac{\Delta I}{2} = \left[\frac{2}{1 - 0.0136} + \frac{3.3\times10^{-3}}{2 \times 125\times10^3 \times 26.0\times10^{-6}}\right] =$$

2.53 A

Peak voltage ratings for the semiconductors:

$$\hat{V}_Q = \hat{V}_D = V_S - V_0 = 400 - (-3.3) = 403.3\ V$$

e) The variation in output voltage at nominal input and if the transistor on time varies by ± 0.008µs:

The transistor on time is:

$$t_1 = \frac{\delta}{f}$$

Where:

$$\delta = \frac{V_O}{V_S + V_O} = \frac{3.3}{320 + 3.3} = 0.0102 \qquad \text{at nominal input}$$

Substitute for δ to obtain:

$$t_1 = \frac{\delta}{f} = \frac{0.0102}{125 \times 10^3} = 0.0817\ \mu s \qquad \text{at nominal input}$$

Therefore the variations in t_1 , δ and V_S will be:

$$t_1 = 0.0817 \pm 0.008\ \mu s$$

$$\delta = t_1 f = (0.0817 \pm 0.008) \times 10^{-6} \times 125 \times 10^3 = 0.0102 \pm 0.001$$

$$V_O = \frac{-\delta V_S}{(1-\delta)} = \frac{-0.0092 \times 320}{(1 - 0.0092)} = -2.97\ \text{V minimum}$$

$$= \frac{-0.0112 \times 320}{(1 - 0.0112)} = -3.62\ \text{V maximum}$$

7.4 SUMMARY OF BASIC CONVERTER EQUATIONS

Parameter	Buck	Boost	Buck - Boost
V_O	δV_S	$\frac{V_S}{(1-\delta)}$	$\frac{-\delta V_S}{(1-\delta)}$
δ	$\frac{V_O}{V_S}$	$\frac{V_O - V_S}{V_S}$	$\frac{V_O}{V_O - V_S}$
ΔI	$\frac{V(1-\delta)}{fL}$	$\frac{V\delta(1-\delta)}{fLN}$	$\frac{V(1-\delta)}{fL}$
ΔV_C	$\frac{V(1-\delta)}{8f^2LC}$	$\frac{I_O\delta}{fC}$	$\frac{I_O\delta}{fC}$
ΔV_R	$\Delta I E_{SR}$	$\left[\frac{I_O}{1-\delta} + \frac{\Delta I}{2}\right]E_{SR}$	$\left[\frac{I_O}{1-\delta} + \frac{\Delta I}{2}\right]E_{SR}$
L_C	$\frac{V(1-\delta)}{2fI_O}$	$\frac{V_O\delta(1-\delta)^2}{2fI_O}$	$\frac{V_O(1-\delta)^2}{2fI_O}$
min. I_O	$\frac{V(1-\delta)}{2fL}$	$\frac{V_O\delta(1-\delta)^2}{2fL}$	$\frac{V_O(1-\delta)^2}{2fL}$
ave. I_L	I_O	$\frac{I_O}{(1-\delta)}$	$\frac{-I_O}{(1-\delta)}$
$\hat{I}_D$, $\hat{I}_Q$, $\hat{I}_L$	$I_O + \frac{\Delta I}{2}$	$\frac{I_O}{1-\delta} + \frac{\Delta I}{2}$	$\frac{-I_O}{1-\delta} + \frac{\Delta I}{2}$
ave. I_Q	δI_O	$\frac{\delta I_O}{(1-\delta)}$	$\frac{-\delta I_O}{(1-\delta)}$
ave. I_D	$(1-\delta)I_O$	I_O	$-I_O$
$\hat{V}_D$, $\hat{V}_Q$	V_S	V_O	$V_S - V_O$

Disadvantages of the basic Buck, Boost, and Buck-boost converters:

a) Output polarity is fixed with respect to input

b) No input/output isolation

Input/output isolation is a safety requirement for all AC input power supplies - UL, CSA, EN, IEC requirements.

Input/output isolation increases noise immunity and reduces noise emissions.

c) Component stresses are maximum

Input and output components are subjected to maximum voltage and maximum current, unlike an AC transformer.

d) Transient variations in δ result in high transients in output voltage especially severe in converters with high V_S/V_O ratio

e) Large V_S/V_O ratio results in very small values for δ and thus maximum values for L_C.

f) Very difficult to get more than one output voltage

All of the above problems can be overcome by using a transformer.
The simplest way to incorporate a transformer in a DC/DC converter is in a bridge configuration. This can be either a Full Bridge or a Half Bridge.

7.5 FULL BRIDGE CONVERTER

The basic schematic diagram of a Full Bridge Converter is shown in **Figure 7.11**.

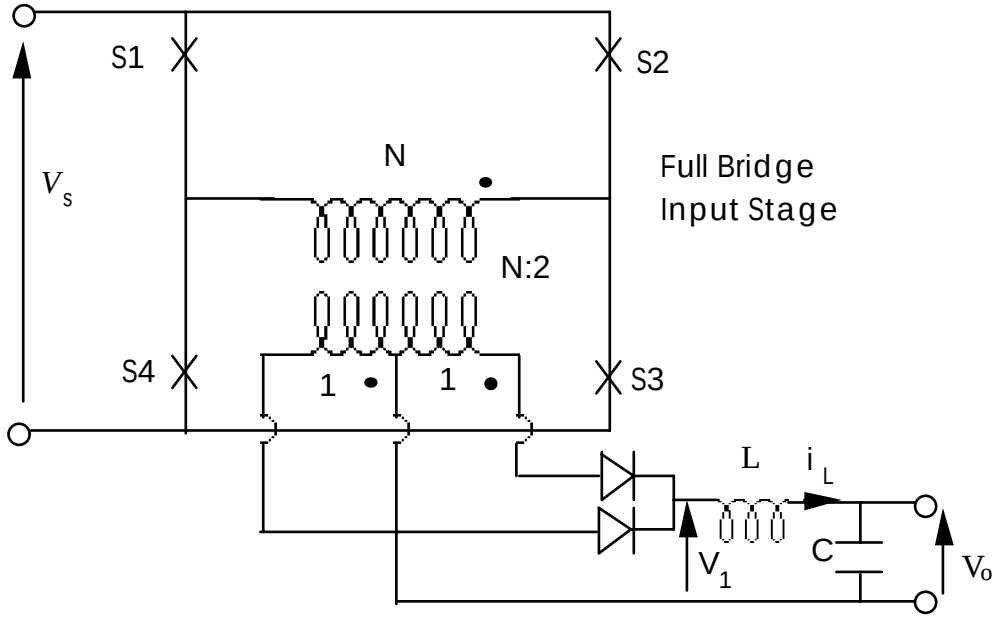


Figure 7.11 Basic Schematic Diagram for a Full Bridge Converter

Switches S1, S2, S3, and S4 form an 'H' bridge which is commonly referred to as Full Bridge. In such a configuration switches S1,S3 and S2,S4 are turned on during alternate half cycles. During each half cycle the active switch pair is on for t_1 seconds and off for t_2 seconds, such that;

$$t_1 + t_2 = \frac{T}{2} = \frac{1}{2f} \qquad (7.5\text{-}1)$$

Also;

$$\delta = \frac{t_1}{T/2} = \frac{2t_1}{T} \qquad (7.5\text{-}2)$$

The basic circuit waveforms for the Full Bridge converter are shown in figure 7.4-2. As can be seen from the waveforms;

$$V_O = \frac{\delta V_S}{N} \qquad (7.5\text{-}3)$$

Therefore the maximum possible value for V_O is:

$$\text{Maximum } V_O = \frac{V_S}{N} \qquad (7.5\text{-}4)$$

$$\text{when } \delta = 1 \qquad (7.5\text{-}5)$$

The Full Bridge converter has all the benefits of transformer isolation that are lacking in basic, transformerless converters, namely;
a) the output voltage can be positive or negative by appropriate configuration of the output diodes.

b) the maximum possible output voltage is limited by the turns ratio
c) even with extreme variations in δ, the output voltage will never exceed a maximum value determined by N.
d) small $\frac{V_O}{V_S}$ ratios can be accommodated by small values of N, without resorting to small values of δ.
e) large $\frac{V_O}{V_S}$ ratios can be accomodated by large values of N, without resorting to small values of δ, as would be required with a Buck-Boost converter.

f) output components are subjected to V_O , I_O , stresses only, and input components are subjected to V_S , I_{in} stresses only, whereas with a transformerless converter all the components would be subjected to the worst of V_O , I_O ,V_S ,I_{in} .
g) multiple outputs can be produced by using multiple secondary windings in the transformer and appropriate diode bridges in each output circuit.

The basic operation of a full bridge converter is similar to that of a buck converter with two exceptions;
a) a transformer with turns ratio N has been inserted between input and output.
b) the frequency in the output stage is doubled

The net result is that the basic equations for a Full Bridge converter are identical to those of a Buck converter with N inserted appropriately and f changed appropriately.

Example Problem 7-4:

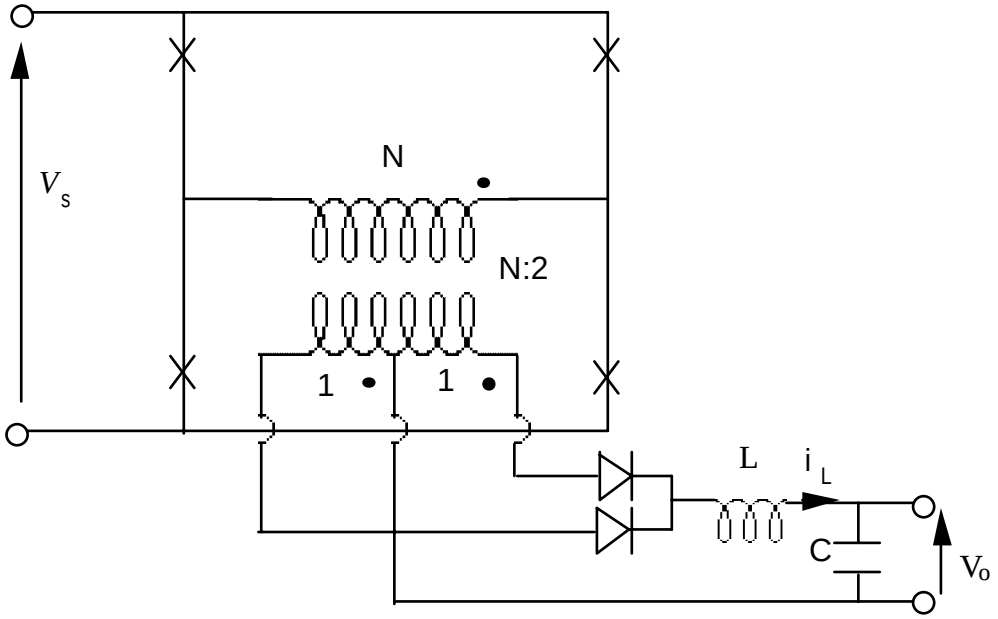
Design a **FULL BRIDGE Converter** to meet the following requirements:

Output voltage: 5 Vdc
Output ripple: 50 mV
Output capacitor: 125 μF
Inductance: 25 μH
Peak Diode current: 22 A, Peak Diode Voltage: 50 V
Peak Transistor current: 2.2 A, Peak Transistor voltage is undetermined
Maximum output current: I_o
Minimum output current: $0.1 \times I_o$

Determine:

a) Transformer turns ratio for maximum utilization of transistors and diodes.
b) Minimum input voltage if maximum duty cycle is 0.95
c) The maximum input voltage and minimum duty cycle.
d) Value of I_o and ΔI.
e) Maximum E_{sr} for the output capacitor.
f) The minimum frequency if ΔV_c is to be less than 50 mV.
g) The peak transistor voltage.

Solution:



Basic circuit diagram for a full bridge converter

a) Transformer turns ratio for maximum utilization of transistors and diodes:

For maximum utilization of the diodes and transistors the transformer turns ratio should be in the inverse ratio as the current ratings for these semiconductors:

$$N = \frac{\hat{I}_D}{\hat{I}_Q} = \frac{22}{2.2} = 10$$

b) Minimum input voltage if maximum duty cycle is 0.95:

$$V_0 = \frac{\delta V_s}{N}$$

Solve for:

$$V_S = \frac{NV_O}{\delta} = \frac{10 \times 5}{0.95} = 52.6 \text{ V}$$

c) The maximum input voltage and minimum duty cycle:

$$\hat{V}_D = \frac{2V_s}{N}$$

Solve for:

$$V_s = \frac{N\hat{V}_D}{2} = \frac{10 \times 50}{2} = 250 \text{ Vdc maximum}$$

Also:

$$\delta = \frac{NV_0}{V_s} = \frac{10 \times 5}{250} = 0.2 \text{ minimum}$$

d) Value of I_o and ΔI:

$$\hat{I}_D = N\hat{I}_Q = I_o + \frac{\Delta I}{2} = 22 \text{ A}$$

And:

$$\Delta I = \frac{V_O(1-\delta)}{2fL}$$

However:

$$I_{min} = \frac{V_O(1-\delta)}{4fL} = \frac{\Delta I}{2} = 0.1 \times I_o$$

Solve for:

$$\Delta I = 0.2 \times I_o$$

Substitute for ΔI into the equation for $\hat{I}_D$ to obtain:

$$\hat{I}_D = I_o + \frac{0.2 \times I_O}{2} = 22 \text{ A}$$

Solve for:

$$I_o = \frac{\hat{I}_D}{1.1} = \frac{22}{1.1} = 20 \text{ A}$$

And:

$$\Delta I = 0.2 \times I_o = 0.2 \times 20 = 4 \text{ A}$$

e) Maximum E_{sr} for the output capacitor:

$$\Delta V_R = \Delta I E_{SR}$$

Solve for:

$$E_{SR} = \frac{\Delta V_R}{\Delta I} = \frac{50}{4} = 12.5\ m\Omega$$

f) The minimum frequency if ΔV_c is to be less than 50 mV:

$$\Delta V_c = \frac{V_O(1-\delta)}{32f^2LC}$$

Solve for:

$$f = \sqrt{\frac{V_O(1-\delta)}{32\Delta V_c LC}} = \sqrt{\frac{5 \times (1 - 0.2)}{32 \times 50\times10^{-3} \times 25\times10^{-6} \times 125\times10^{-6}}} = 28.3$$

kHz

g) The peak transistor voltage:

$$\hat{V}_Q = V_s = 250\ V$$

Comparison of equations for Buck and Full Bridge Converters

Parameter	Buck Converter	Full Bridge Primary	Full Bridge Secondary
V_O	δV_S	–	$\frac{\delta V_S}{N}$
δ	$\frac{V_O}{V_S}$	–	$\frac{NV_O}{V_S}$
ΔI	$\frac{V(1-\delta)}{fL}$	$\frac{V(1-\delta)}{2fLN}$	$\frac{V(1-\delta)}{2fL}$
ΔV_C	$\frac{V(1-\delta)}{8f^2LC}$	–	$\frac{V(1-\delta)}{32f^2LC}$
ΔV_R	ΔIE_{SR}	–	ΔIE_{SR}
L_C	$\frac{V(1-\delta)}{2fI_O}$	–	$\frac{V(1-\delta)}{4fI_O}$
min. I_O	$\frac{V(1-\delta)}{2fL}$	–	$\frac{V(1-\delta)}{4fL}$
ave. I_L	I_O	$\frac{I_O}{N}$	I_O
$\hat{I}_D, \hat{I}_Q$	$I_O + \frac{\Delta I}{2}$	$\frac{I_O + \frac{\Delta I}{2}}{N}$	$I_O + \frac{\Delta I}{2}$
ave. I_Q	δI_O	$\frac{\delta I_O}{2N}$	–
ave. I_D	$(1-\delta)I_O$	–	$\frac{I_O}{2}$
$\hat{V}_D, \hat{V}_Q$	V_S	V_S	$\frac{2V_S}{N}$

7.6 HALF BRIDGE CONVERTER

The basic schematic diagram of a Half Bridge Converter is shown in **Figure 7.12**.

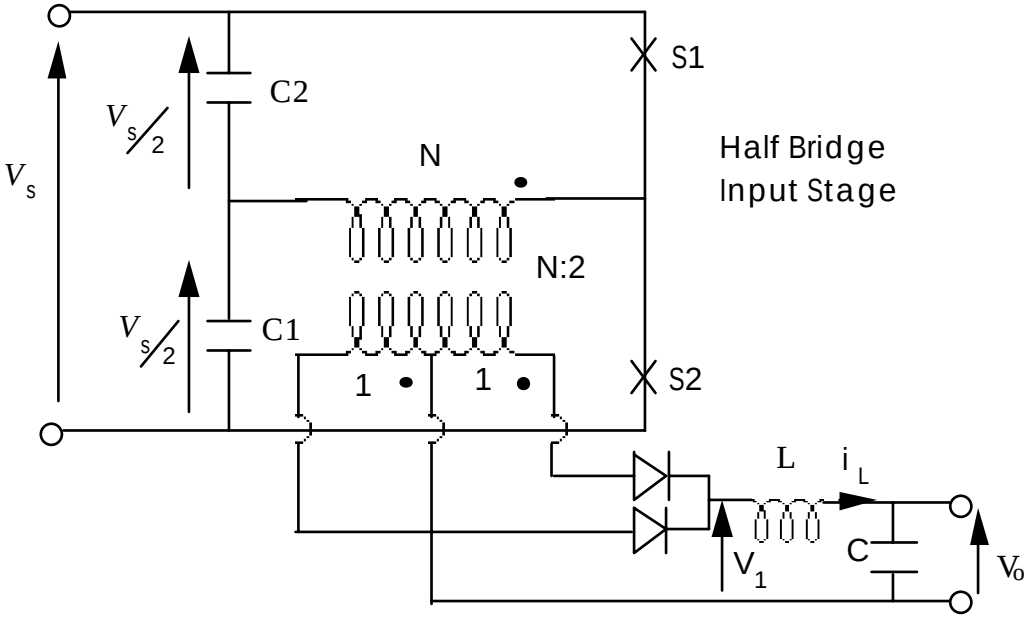


Figure 7.12 Basic Schematic Diagram for a Half Bridge Converter

Switches S1 and S2 form half of an 'H' bridge, and capacitors C1and C2 form the other half. This is commonly referred to as a Half Bridge. In such a configuration switches S1 and S2 are turned on during alternate half cycles. During each half cycle the active switch is on for t_1 seconds and off for t_2 seconds, such that;

$$t_1 + t_2 = \frac{T}{2} = \frac{1}{2f} \qquad (7.6\text{-}1)$$

Also;

$$\delta = \frac{t_1}{T/2} = \frac{2t_1}{T} \qquad (7.6\text{-}2)$$

Capacitors C1, C2 are chosen such that C1 = C2 = C and the voltage swing across each capacitor is negligible compared to the input voltage V_S .

The basic circuit waveforms for the Half Bridge converter are shown in figure 7.6-2. As can be seen from these waveforms;

$$V_O = \frac{\delta V_S}{2N} \qquad (7.6\text{-}1)$$

The Half Bridge converter has all the benefits of transformer isolation that the Full Bridge converter had, namely;

a) the output voltage can be positive or negative by appropriate configuration of the output diodes.

b) the maximum possible output voltage is limited by the turns ratio

c) even with extreme variations in δ, the output voltage will never exceed a maximum value determined by N.

d) small $\frac{V_O}{V_S}$ ratios can be accommodated by small values of N, without resorting to small values of δ.

e) large $\frac{V_O}{V_S}$ ratios can be accommodated by large values of N, without resorting to small values of δ, (as would be required with a Buck-Boost converter.

f) output components are subjected to V_O, I_O, stresses only, and input components are subjected to V_S, I_{in} stresses only, whereas with a transformerless converter all the components would be subjected to the worst of V_O, I_O, V_S, I_{in}.

g) multiple outputs can be produced by using multiple secondary windings in the transformer and appropriate diode bridges in each output circuit.

The net result is that the basic equations for a Half Bridge converter are generally identical to those of a Full Bridge converter with V_S reduced by 1/2.

The only exception is that the peak transistor voltage, $\hat{V}_Q$, is the same for both the half bridge and full bridge converters:

$\hat{V}_Q = V_S$ for both half bridge and full bridge converters

Half Bridge Converter with AC Input

A very common application for Half Bridge converters is in AC to DC power supplies in which the AC input is rectified to produce the V_S input voltage to a Half Bridge converter as shown in **Figure 7.13**.

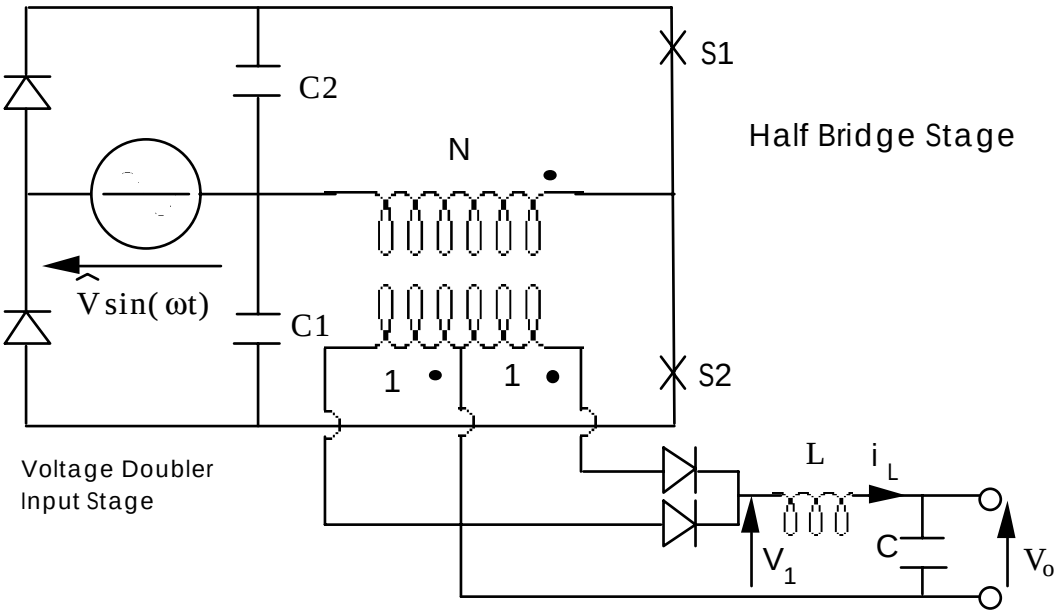


Figure 7.13 Half Bridge Converter With an AC input

Capacitors C1 and C2 are required to filter out the AC ripple in the resultant rectified waveform in order to produce a relatively smooth DC waveform for V_S. Thus a half bridge converter is very economical for AC input power supplies because the input capacitors are required anyways for filtering the AC ripple.

In the particular case of the voltage doubler circuit shown in **Figure 7.13**, the capacitors are required not only for filtering but also to produce the voltage double effect. Thus a half bridge converter, when used with AC input power supplies, effectively gets the input capacitors C1 and C2 for "free".

Example Problem 7-5

You have to design a **Half Bridge converter** to produce a 5V output using the following components:

Output capacitor: C = 6000μF, E_{SR} = 10 mΩ

Inductor: L = 5.5 μH

Diode: 150 V, 30 A peak

Transistor: 400V, 6 A peak

Switching frequency: 200 kHz,

Transformer turns ratio 4:1 for input:output.

a) Draw the basic circuit diagram, and determine:

b) The maximum input voltage and the corresponding duty cycle.

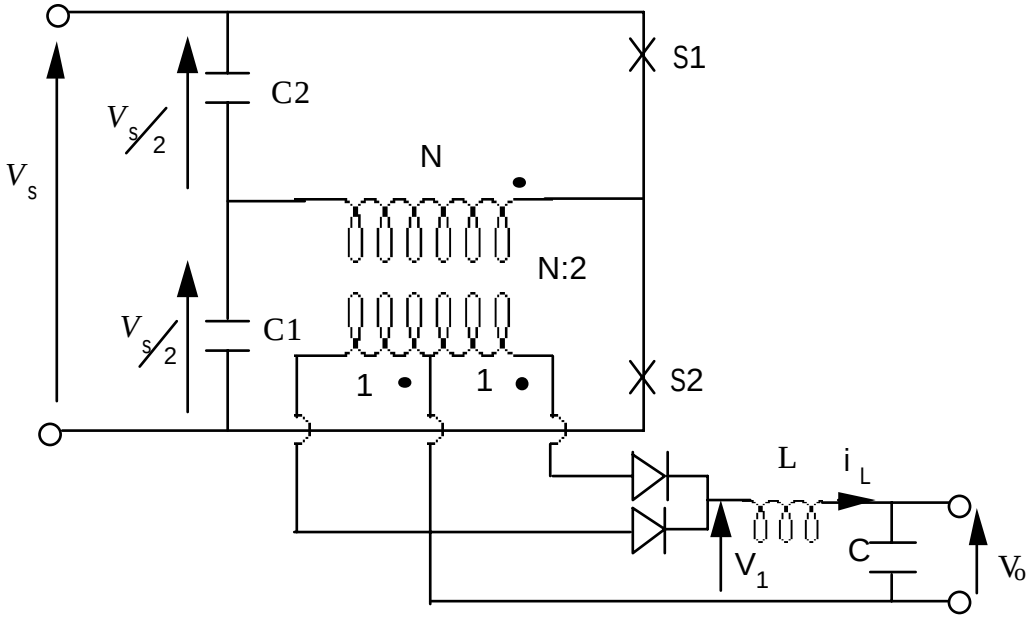
c) The minimum input voltage if maximum duty cycle is 0.95.

d) The minimum load current.

e) The worst case ΔI.

Solutions:

a) Basic circuit diagram:



b) The maximum allowable input voltage and the corresponding duty cycle, if the output voltage is to be 5V:

$$\hat{V}_Q = V_S$$

Therefore:

$$V_S = \hat{V}_Q = 400 \text{ V}$$

Also:

$$\hat{V}_D = \frac{V_S}{N}$$

Solve for:

$$V_S = N\hat{V}_D = 4 \times 150 = 600 \text{ V}$$

Therefore the maximum input voltage will be 400 volts limited by the transistor rating.
Also:

$$V_0 = \frac{\delta V_S}{2N}$$

Thus the corresponding duty cycle will be:

$$\delta = \frac{2NV_0}{V_s} = \frac{2 \times 4 \times 5}{400} = 0.1$$

c) The minimum input voltage if maximum duty cycle is 0.95:

$$V_S = \frac{2NV_O}{\delta} = \frac{2 \times 4 \times 5}{0.95} = 42.1 \text{ V}$$

d) The minimum load current:

$$I_{min} = \frac{V_O(1-\delta)}{4fL} = \frac{5 \times (1 - 0.1)}{4 \times 200\times10^3 \times 5.5\times10^{-3}} = 1.03 \text{ mA}$$

e) The worst case ΔI:

$$\Delta I = \frac{V_O(1-\delta)}{2fL} = \frac{5 \times (1 - 0.1)}{2 \times 200\times10^3 \times 5.5\times10^{-3}} = 2.05 \text{ mA on secondary side}$$

f) The maximum output current:

$$\hat{I}_D = I_0 + \frac{\Delta I}{2}$$

Solve for:

$$I_0 = \hat{I}_D - \frac{\Delta I}{2} = 30 - \frac{0.00205}{2} = 29.999 \text{ A} = 30 \text{ A}$$

Similarly:

$$\hat{I}_Q = \frac{I_0}{N} + \frac{\Delta I}{2N}$$

Solve for:

$$I_0 = N\left[\hat{I}_Q - \frac{\Delta I}{2}\right] = 4 \times \left[6 - \frac{0.00205}{2}\right] = 24 \text{ A}$$

Therefore the maximum output current will be 24 A, limited by the transistor rating.
g) The worst case output ripple:

$$\Delta V_c = \frac{V_O(1-\delta)}{32f^2LC} = \frac{5 \times (1 - 0.1)}{32 \times \left[200\times10^3\right]^2 \times 5.5\times10^{-3} \times 6000\times10^{-6}} = 0.107 \text{ } \mu\text{V}$$

Also:

$$\Delta V_R = \Delta I E_{SR} = 2.05\times10^{-3} \times 10\times10^{-3} = 20.5 \text{ } \mu\text{V}$$

Thus the worst case ripple will be 20.5 µV due to ΔV_R

Comparison of Buck and Full Bridge and Half Bridge Converters

Parameter	Buck Converter	Full Bridge Converter	Half Bridge Converter
V_O	δV_S	$\frac{\delta V_S}{N}$	$\frac{\delta V_S}{2N}$
δ	$\frac{V_O}{V_S}$	$\frac{NV_O}{V_S}$	$\frac{2NV_O}{V_S}$
primary ΔI	$\frac{V(1-\delta)}{fL}$	$\frac{V(1-\delta)}{2fLN}$	$\frac{V(1-\delta)}{2fLN}$
ΔV_C	$\frac{V(1-\delta)}{8f^2LC}$	$\frac{V(1-\delta)}{32f^2LC}$	$\frac{V(1-\delta)}{32f^2LC}$
ΔV_R	ΔIE_{SR}	ΔIE_{SR}	ΔIE_{SR}
L_C	$\frac{V(1-\delta)}{2fI_O}$	$\frac{V(1-\delta)}{4fI_O}$	$\frac{V(1-\delta)}{4fI_O}$
min. I_O	$\frac{V(1-\delta)}{2fL}$	$\frac{V(1-\delta)}{4fL}$	$\frac{V(1-\delta)}{4fL}$
ave. I_L	I_O	I_O	I_O

Comparison of Buck and Full Bridge and Half Bridge Converters (cont'd)

Parameter	Buck Converter	Full Bridge Converter	Half Bridge Converter
$\hat{I}_Q$	$I_O + \frac{\Delta I}{2}$	$\frac{I_O + \frac{\Delta I}{2}}{N}$	$\frac{I_O + \frac{\Delta I}{2}}{N}$
$\hat{I}_D$	$I_O + \frac{\Delta I}{2}$	$I_O + \frac{\Delta I}{2}$	$I_O + \frac{\Delta I}{2}$
ave. I_Q	δI_O	$\frac{\delta I_O}{2N}$	$\frac{\delta I_O}{2N}$
ave. I_D	$(1-\delta)I_O$	$\frac{I_O}{2}$	$\frac{I_O}{2}$
$\hat{V}_Q$	V_S	V_S	V_S
$\hat{V}_D$	V_S	$\frac{2V_S}{N}$	$\frac{V_S}{N}$
Switches	1	4	2
Diodes	1	2	2
H.V. Capacitors	–	–	2

7.7 PUSH-PULL CONVERTER

A common type of converter used for low input voltage applications is called a push-pull converter. The basic circuit diagram for such a converter is shown in **Figure 7.14**.

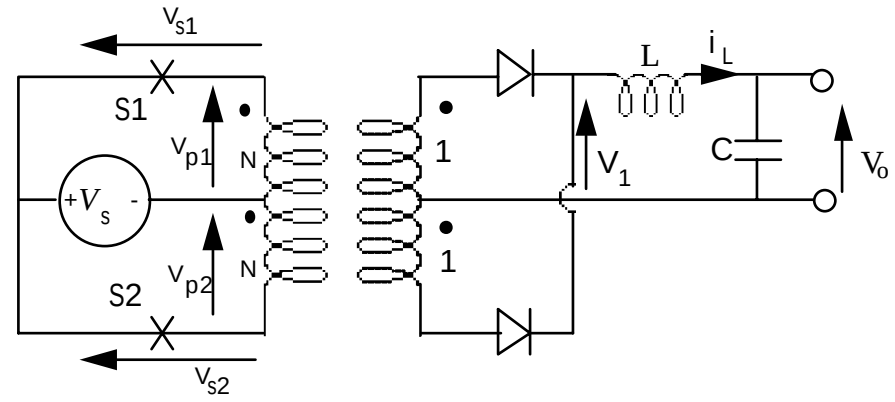


Figure 7.14 Basic Schematic Diagram for a Push-Pull Converter

Switches S1and S2 are turned on during alternate half cycles. During each half cycle the active switch is on for t_1 and off for t_2 seconds.

Therefore:

$$t_1 + t_2 = \frac{T}{2} = \frac{1}{2f} \qquad (7.7\text{-}1)$$

Also;

$$\delta = \frac{t_1}{T/2} = \frac{2t_1}{T} \qquad (7.7\text{-}2)$$

Note that the output stage of a push-pull converter is identical to that of a full and/or half bridge converter. Also, a push-pull converter only requires two primary switches and does not require an input capacitor, except for filtering.

The operation of a push-pull converter is similar to that of a bridge converter except that when each switch is "on" the complementary "off" switch sees double the input voltage, V_s. The operation of the secondary side is identical to that of the half bridge and full bridge converters.

Example Problem 7-6

You have to use a **PUSH-PULL Converter** that was designed with the following components and constraints:

Output capacitor: C = 6000μF, E_{SR} = 10 mΩ

Transformer: N = 4, L = 5.5 mH

Diodes: 150 V, 30 A peak

Transistors: 400V, 6 A peak

Switching frequency: 200 kHz, Duty cycle: 0.8 maximum

a) Draw the basic circuit diagram.

b) If the output voltage is to be 5V, what would be the maximum allowable input voltage and the corresponding duty cycle.

c) What is the minimum input voltage if maximum duty cycle is still 0.8.

d) What is the minimum load current.

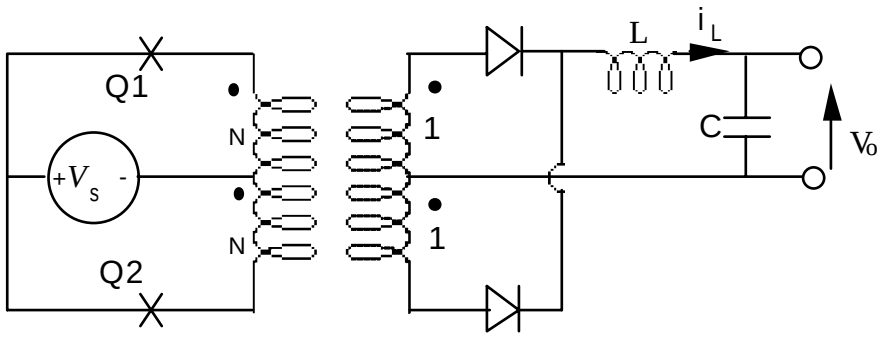
e) What is worst case ΔI.

f) What is the maximum output current.

g) What is the worst case output ripple.

Solution:

a) Basic circuit diagram:



b) If the output voltage is to be 5V, what would be the maximum allowable input voltage and the corresponding duty cycle:

$$\hat{V}_Q = 2V_S$$

Therefore:

$$V_S = \frac{\hat{V}_Q}{2} = \frac{400}{2} = 200 \text{ V}$$

$$\hat{V}_D = \frac{2V_S}{N}$$

Solve for:

$$V_S = \frac{N\hat{V}_D}{2} = \frac{4 \times 150}{2} = 300 \text{ V}$$

Therefore the maximum input voltage will be 200 volts limited by the transistor rating.

Also the corresponding duty cycle will be:

$$\delta = \frac{NV_0}{V_s} = \frac{4 \times 5}{200} = 0.1$$

c) What is the minimum input voltage if maximum duty cycle is still 0.8:

$$V_S = \frac{NV_O}{\delta} = \frac{4 \times 5}{0.8} = 25 \text{ V}$$

d) What is the minimum load current:

$$I_{min} = \frac{V_O(1-\delta)}{4fL} = \frac{5 \times (1 - 0.1)}{4 \times 200\times10^{3} \times 5.5\times10^{-3}} = 1.02 \text{ mA}$$

e) What is worst case ΔI:

$$\Delta I = \frac{V_O(1-\delta)}{2fL} = \frac{5 \times (1 - 0.1)}{2 \times 200\times10^{3} \times 5.5\times10^{-3}}$$

$= 2.04$ mA on secondary side

f) What is the maximum output current:

$$\hat{I}_D = I_0 + \frac{\Delta I}{2}$$

Solve for:

$$I_0 = \hat{I}_D - \frac{\Delta I}{2} = 30 - \frac{0.00204}{2} = 29.999 \text{ A} = 30 \text{ A}$$

Similarly:

$$\hat{I}_Q = \frac{I_0}{N} + \frac{\Delta I}{2N}$$

Solve for:

$$I_0 = N\left[\hat{I}_Q - \frac{\Delta I}{2}\right] = 4 \times \left[6 - \frac{0.00204}{2}\right] = 24 \text{ A}$$

Therefore the maximum output current will be 24 A, limited by the transistor rating.

g) What is the worst case output ripple:

$$\Delta V_c = \frac{V_O(1-\delta)}{32f^2LC} = \frac{5 \times (1 - 0.1)}{32 \times \left[200\times10^{3}\right]^2 \times 5.5\times10^{-3} \times 6000\times10^{-6}}$$

$= 1.07 \ \mu V$

Also:

$$\Delta V_R = \Delta I E_{SR} = 2.04\times10^{-3} \times 10\times10^{-3} = 20.4 \ \mu V$$

Thus the worst case ripple will be 20.4 μV due to E_{SR}

Comparison of Full Bridge and Push-Pull Converters

Parameter	Full Bridge Converter primary	Full Bridge Converter secondary	Push-Pull Converter primary	Push-Pull Converter secondary
V_O		$\frac{\delta V_S}{N}$		$\frac{\delta V_S}{N}$
ΔI	$\frac{V_O(1-\delta)}{2fLN}$	$\frac{V_O(1-\delta)}{2fL}$	$\frac{V_O(1-\delta)}{2fLN}$	$\frac{V_O(1-\delta)}{2fL}$
peak V_Q V_D	V_S	$\frac{2V_S}{N}$	$2V_S$	$\frac{2V_S}{N}$
Switches	4	—	2	—
Diodes	—	2	—	2

7.8 FLYBACK CONVERTER

The full/half bridge and push-pull converters are basically buck converters with transformers. A buck-boost converter with a transformer is called a flyback converter. The basic schematic diagram for a flyback converter is shown in **Figure 7.15**.

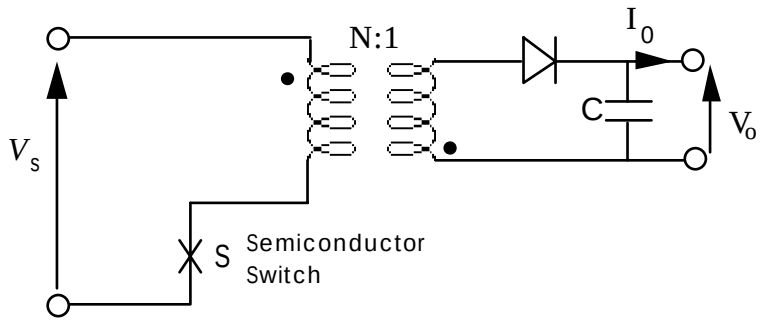


Figure 7.15 Basic Schematic Diagram for a Flyback Converter

The output is isolated from the input and can be positive or negative by appropriate diode configuration. It is significant to note that the circuit of **Figure 7.15** does not show an inductor. The flyback converter, like the buck-boost converter from which it is derived, does utilize an inductor. However the magnetizing inductance of the transformer is used as the energy storage inductor in a Flyback Converter as shown in **Figure 7.16**.

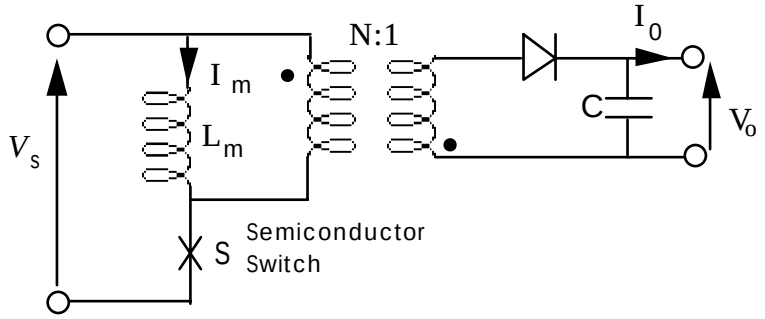


Figure 7.16 Flyback Converter Circuit Including Transformer Magnetizing Inductance

Switch S is on for t_1 seconds and off for t_2 seconds.

Therefore:

$$t_1 + t_2 = T = \frac{1}{f} \qquad (7.8\text{-}1)$$

Also;

$$\delta = \frac{t_1}{T} \qquad (7.8\text{-}2)$$

When the switch S is turned on at t=0, the output voltage of the transformer is configured such that diode D becomes reverse biased and acts as an open

circuit. This is referred to a Mode I and the equivalent circuit for this mode is shown in **Figure 7.17**.

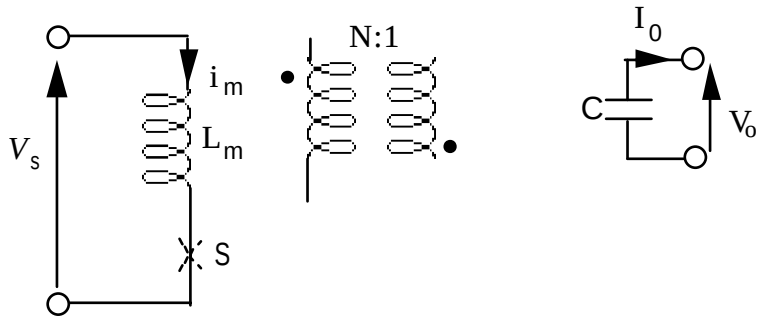


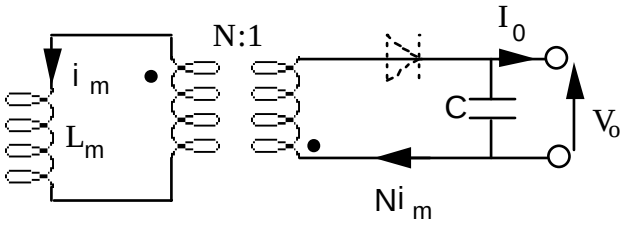
Figure 7.17 Equivalent Circuit During Mode I

This equivalent circuit is identical to the Mode I equivalent circuit for a Buck-boost converter as shown in **Figure 7.9**.

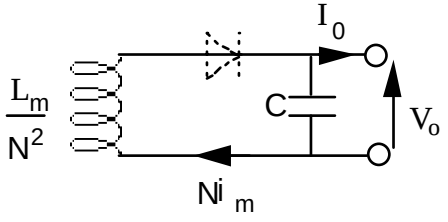
The current, i_m , through the magnetizing inductance will be the same as the inductor current in the Buck-boost analysis of **Section 7.3**:

$$i_m(t) = I_1 + \frac{V_S t}{L} \qquad (7.8\text{-}3)$$

When the switch S is opened at $t=t_1$, the circuit reverts to Mode II. The equivalent circuit for this mode is shown in **Figure 7.18**.



a) With Magnetizing inductance on the primary side



b) Magnetizing inductance reflected to the secondary side

Figure 7.18 Equivalent Circuit During Mode II

The inductor current at $t=t_1$ is:

$$i_m(t_1) = I_1 + \frac{V_S t_1}{L} = I_2 \qquad (7.8\text{-}4)$$

This current cannot go to zero instantaneously and instead it circulates through the transformer as shown in **Figure 7.18** and into the output circuit. The diode becomes forward biased and conducts. On the secondary side the magnetizing current becomes, i'_m , where:

$$i'_m = Ni_m \qquad (7.8\text{-}5)$$

The equations for a flyback converter in Mode II are similar to those of a buck-boost converter in Mode II except that the output current, voltage and inductance have been reflected through a transformer of turns ratio N.

It is important to note that the flyback converter combines the inductor and transformer into one magnetic device. This is called "integrated magnetics". The flyback converter also provides transformer isolation with only one switch. This is a very economical converter circuit, especially at low power levels (less than 100W). The flyback converter is used in every TV and video monitor to produce the high voltage for CRT deflection.

Example Problem 7-7

Design a **FLYBACK DC/DC converter** to meet the following requirements:

Input Voltage, V_{in} = 320 ± 80 Vdc

Output Voltage, V_o = 3.3Vdc with a maximum ripple of 30mV p-p.

Output Current, I_o = 0.5 A minimum, 2.0 A maximum.

Switching frequency f = 125 kHz

Determine the following:

a) The transformer turns ratio, assuming a maximum duty cycle of 0.55

b) The duty cycle at minimum and maximum input voltage

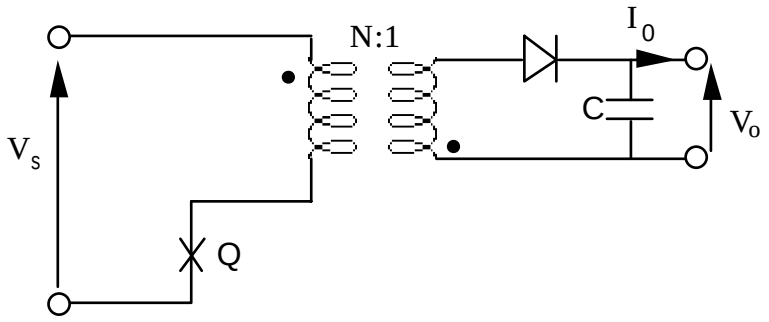
c) The critical inductance, referred to the **primary** side.

d) The minimum number of output capacitors if each capacitor has 1,000 µF and and an E_{sr} of 10 mΩ.

e) The peak current and voltage ratings for the semiconductors.

f) The variation in output voltage at nominal input and if the transistor on time varies by ± 0.008µs:

Solution:



Basic circuit diagram for a flyback converter

a) The transformer turns ratio, assuming a maximum duty cycle of 0.55:

$$V_O = \frac{\delta V_S}{N(1-\delta)}$$

Solve for:

$$N = \frac{\delta V_S}{V_O(1-\delta)} = \frac{0.55 \times (320 - 80)}{3.3 \times (1 - 0.55)} = 88.9$$

b) Duty cycle at min and max input voltage:

$$\delta = \frac{NV_O}{V_S + NV_O} = \frac{88.9 \times 3.3}{240 + 88.9 \times 3.3} = 0.550 \text{ @ minimum } V_S$$

$$= \frac{88.9 \times 3.3}{400 + 88.9 \times 3.3} = 0.423 \text{ @ maximum } V_S$$

c) The critical inductance, referred to the **primary** side:

$$L_c = \frac{V_O(1-\delta)^2}{2fI_O} = \frac{3.3 \times (1 - 0.423)^2}{2 \times 125 \times 10^3 \times 0.5} = 8.79 \text{ µH on the secondary side}$$

On the primary side:

$$L_c = N^2 L_c = 88.9^2 \times 8.79\times10^{-6} = 69.4 \text{ mH}$$

d) The minimum number of output capacitors if each capacitor has 1,000 μF and an E_{sr} of 10 mΩ:

$$\Delta V_C = \frac{I_O \delta}{fC}$$

Solve for:

$$C = \frac{I_O \delta}{f \Delta V_C} = \frac{2 \times 0.550}{125\times10^3 \times 30\times10^{-3}} = 293 \text{ μF}$$

Therefore one 1,000 μF capacitor would be required if ΔV_C were the determining criteria.

Also:

$$\Delta V_R = \left[\frac{I_0}{1-\delta} + \frac{\Delta I}{2}\right] E_{SR}$$

Where:

$$\Delta I = \frac{V_O(1-\delta)}{fL_m}$$

Substitute for ΔI to obtain:

$$E_{SR} = \frac{\Delta V_R}{\left[\frac{I_0}{1-\delta} + \frac{\Delta I}{2}\right]}$$

$$= \frac{\Delta V_R}{\left[\frac{I_0}{1-\delta} + \frac{V_O(1-\delta)}{2fL_m}\right]} = \frac{30\times10^{-3}}{\left[\frac{2}{1 - 0.550} + \frac{3.3 \times (1 - 0.550)}{2 \times 125\times10^3 \times 8.79\times10^{-6}}\right]} =$$

5.86 mΩ

Therefore two 1,000 μF capacitor would be required if ΔV_R were the determining criteria.

Therefore the correct number of capacitors is 2.

e) The peak current and voltage ratings for the semiconductors:

$$\hat{I}_D = \frac{I_0}{1-\delta} + \frac{\Delta I}{2} = \left[\frac{2}{1 - 0.550} + \frac{3.3 \times (1 - 0.550)}{2 \times 125\times10^3 \times 8.79\times10^{-6}}\right] = 5.12 \text{ A}$$

$$\hat{I}_Q = \frac{\hat{I}_D}{N} = \frac{5.12}{88.9} = 57.6 \text{ mA}$$

Peak voltage ratings for the semiconductors:

$$\hat{V}_Q = V_S + NV_0 = 400 + 88.9 \times 3.3 = 693 \text{ V}$$

$$\hat{V}_D = \frac{V_S}{N} + V_0 = \frac{400}{88.9} + 3.3 = 7.80 \text{ V}$$

f) The variation in output voltage at nominal input and if the transistor on time varies by ± 0.008μs:

The transistor on time is:

$$t_1 = \frac{\delta}{f}$$

Where:

$$\delta = \frac{NV_O}{V_S + NV_O} = \frac{88.9 \times 3.3}{320 + 88.9 \times 3.3} = 0.478 \text{ at nominal input}$$

Substitute for δ to obtain:

$$t_1 = \frac{\delta}{f} = \frac{0.478}{125 \times 10^3} = 3.83 \text{ μs at nominal input}$$

Therefore the variations in t_1, δ and V_O will be:

$$t_1 = 3.83 \pm 0.08 \text{ μs}$$

$$\delta = t_1 f = = (3.83 \pm 0.008) \times 10^{-6} \times 125 \times 10^3 = 0.478 \pm 0.001$$

$$V_O = \frac{\delta V_S}{N(1-\delta)} = \frac{0.477 \times 320}{88.9 \times (1 - 0.477)} = 3.28 \text{ V minimum}$$

$$= \frac{0.479 \times 320}{88.9 \times (1 - 0.479)} = 3.31 \text{ V maximum}$$

Comparison of Buck-Boost and Flyback Converters

	Buck-Boost	Flyback Converter	
Error!			
average I_L	$\frac{I_O}{1-\delta}$	$\frac{I_O}{N(1-\delta)}$	$\frac{I_O}{1-\delta}$
$\hat{I}_L$	$\frac{I_O}{1-\delta} + \frac{\Delta I}{2}$	$\frac{I_O}{N(1-\delta)} + \frac{\Delta I}{2}$	$\frac{I_O}{1-\delta} + \frac{\Delta I}{2}$
$\hat{I}_Q, \hat{I}_D$	$\frac{I_O}{1-\delta} + \frac{\Delta I}{2}$	$\frac{I_O}{N(1-\delta)} + \frac{\Delta I}{2}$	$\frac{I_O}{1-\delta} + \frac{\Delta I}{2}$
$\hat{V}_Q, \hat{V}_D$	$V_S + V_O$	$V_S + NV_O$	$\frac{V_S}{N} + V_O$

7.9 PRECAUTIONS WITH SWITCHED MODE POWER SUPPLIES

Switched mode power supplies, (also known as SMPS, switchers and SMR's), have inherent problems which should be appreciated and adressed if they are to be used effectively in any particular application:

a) Output Filtering

Regardless of how large the output capacitor is or how low its E_{SR} is there will always be "switching spikes" in the output waveform. These spikes get onto the output due to parasitic capacitances in the output inductor that conduct high frequency components of the switching pulses. These spikes can best be eliminated by using "decoupling" capacitors at the "load" circuitry.

b) Input Filtering

Many power supplies are sold with little or no input filter capacitors. This can result in high levels of radiated noise and could even damage the power supply (and other circuitry) if the source voltage has significant inductance.

c) Heat

Switching power supplies are much smaller than "linear" power supplies but they still dissipate heat, often at a much higher volumetric density than linear power supplies. They will overheat if cooling, (air flow), is inadequate. Many so-called high density power supplies are sold on the assumption that an external heat sink and cooling system will be added when in use.

d) Ambient Temperature

All electronic components and circuits including power supplies have an inherent maximum operating temperature beyond which the circuit will not operate properly and/or components may be damaged. For most power supplies that dissipate a lot of heat the actual operating temperature of the power supply may be significantly higher than the "room ambient". For example a stereo system may operate in a room temperature of 25°C but if the power supply inside it is inadequately cooled its temperature may reach 85°C which is beyond the range of most "commercial grade" components.

e) Minimum Load

Most switching power supplies have a minimum load requirement that often isn't advertised by the manufacturer. If the power supply is operated below its minimum load the output ripple will be higher than expected and may even cause the power supply to shut down.

f) Inrush Current

If the power supply input filter consists of just a large capacitor then it may draw very high currents everytime input voltage is applied. This may cause fuses and circuit breakers to trip and/or overstress components. Such power supplies may require additional inrush current limiting circuitry.

g) Overvoltage Protection

This is required to ensure that even if the power supply malfunctions it will still not produce an excessively high output voltage that could damage "downstream" circuitry. The overvoltage protection should be independent of the normal control circuitry.

h) Output Current Limit, Current Foldback.

This is required to ensure that the power supply does not overheat (and cause fire, or other safety hazards) when the output is overloaded or shorted. Firstly the power supply must survive a permanent overload on its output. Secondly the "downstream" circuitry must be designed such that it too will survive a high current condition. One way to achieve this is to design the power supply such that if there is a short circuit on the output the power supply current "folds back" to a lower and safer value.

I) Undervoltage Shutdown

This is required to ensure that the power supply doesn’t destroy itself (or cause a fire/shock hazard) if an internal component fails.

j) AC Outage and Transient Behaviour

If the power supply is fed from commercial AC then it has to be protected against high and low transients and should have graceful shut down in the event of AC failure, with automatic restart when the AC recovers. It is often useful to have "hold-up" capacitors to ride out short duration AC outages, (up to 100 milliseconds).

k) Safety

All AC input power supplies should be approved by independent safety agencies. In Canada the agency is CSA, (Canadian Standards Association), and in the US it is UL, (Underwriter’s Laboratories). To meet their safety requirements power supplies generally must demonstrate:

- input output isolation, typically to 1500V
- short circuit protection
- internal fault tolerance resulting in no hazard

- no thermal or electrical overstressing of critical components

l) Input Current and Voltage Distortion

For many AC input switched mode power supplies the input current is very "peaky" due to the input capacitors which only charge up during a narrow conduction interval during each AC half cycle. This results in:

- high rms ripple currents on the input which can lead to overheating of input components
- high crest factors, where the crest factor, CF is defined as

  $CF = \frac{\hat{I}}{I_{rms}}$ Note that for a pure sine wave CF = 1.414
- high levels of third, ninth, fifteenth harmonics which are additive in three phase neutral wires and can result in overheating of the neutral wire
- distortion of the input voltage waveform, creating high levels of voltage harmonics which may cause excessive magnetizing losses in other devices connected to the same voltage source

The problems associated with input current/voltage distortion can be avoided by "unity power factor" circuits which is usually another power supply in front of the "main" power supply.

7.10 PROBLEMS

7.10.1 Buck Converters

1. Design a Buck Converter to meet the following requirements;

Vs=320±50Vdc,
V_O =50Vdc,
Maximum ripple=150 mV p-p,
I_O =5A minimum, 50A maximum,
Switching frequency is 120kHz.

Draw the equivalent circuit and determine:
a)The minimum duty cycle and under what conditions it occurs. (0.135)
b)The minimum inductance required and the worst case average and peak current rating for this inductor. (36µH, 50A average, 55A peak)
c)The output capacitance required assuming E_{SR} =0. (69.4ΩF)
d)The output capacitance required assuming E_{SR} =50mΩ/1000µF. (4,000µF)
e)The peak voltage and peak current ratings for the semiconductors. (370V, 55A)

2. Design a Buck Converter to operate from a 12V (nominal) car battery. The requirements are;

Input Voltage: 10.5 Vdc to 15.9 Vdc
Output Current: 0.5A to 1.5A
Output Voltage: 5 Vdc
Output Ripple: 25mVp-p
Switching Frequency: 250kHz

Determine;
a)The minimum and maximum duty cycle and under what conditions each occurs. (0.314, 0.476)
b)The critical inductance. (13.7µH)
c)The output capacitance assuming E_{SR} =0. (126µF)
d)The output capacitance assuming E_{SR} =50mΩ/1000µF. (2,000µF)
e)The peak voltage and peak current ratings for the semiconductors. (15.9V, 2.5A)

7.10.2 Boost Converters

3. You are given a **BOOST CONVERTER** with the following characteristics:

V_S = 5 V, V_O = 20 V, output C = 100 µF (E_{SR} = 0),

ΔV_C = 250 mV at I_O = 1.0 A

Inductor current goes to zero at I_O = 0.1 A

Determine:

a) The duty cycle, δ. (0.75)

b) The switching frequency, f. (30kHz)

c) The inductance, L. (156µH)

7.10.3 Buck-Boost Converters

4. Design a DC/DC Converter to meet the following requirements;

Input Voltage, V_S =150±50Vdc,

Output Voltage, V_o =-150Vdc,

Output Current, I_o =5A minimum, 50A maximum,

You are given one transistor, one diode, a capacitor of 4700µF, an inductor of 25µH and no transformer.

Determine:

a)The minimum and maximum duty cycle and under what conditions each occurs. (0.423, 0.600)

b)The minimum switching frequency to keep inductor current from going to zero. (196kHz)

c)The minimum switching frequency to keep the output ripple within 75 mV p-p. (85.1kHz)

d)The peak voltage and peak current ratings for the semiconductors if the switching frequency is 200KHz. (350V, 127.4A)

7.10.4 Full-Bridge Converters

5. Design a Full Bridge Converter to meet the following requirements;

V_S =320±50Vdc,

V_O =50Vdc,

Maximum ripple=150 mV p-p,

I_O =5A minimum, 50A maximum,

Switching frequency is 120kHz.

Determine:

a)The transformer turns ration such that the maximum duty cycle does not exceed 95%. (5.13)

b)The minimum duty cycle and under what conditions it occurs. (0.69)

c)The minimum inductance required and the worst case average and peak current rating for this inductor. (6.46µH, 50A average, 55A peak)

d)The output capacitance required assuming E_{SR} =0. (34.7µF)

e)The output capacitance required assuming E_{SR} =50mΩ/1000µF. (4,000µF)

f)The peak voltage and peak current ratings for the semiconductors. (370V, 10.7A, 144V, 55A)

6. Design a Full Bridge Converter to meet the following requirements;

V_S =300±50Vdc,

V_O =50Vdc,

Maximum ripple=200 mV p-p,

I_O =1A minimum, 25A maximum,

Switching frequency is 200kHz.

Determine:

a)The transformer turns ration such that the maximum duty cycle does not exceed 99%. (4.95)

b)The minimum duty cycle and under what conditions it occurs. (0.707)

c)The minimum inductance required and the worst case average and peak current rating for this inductor. (18.3µH, 25A average, 26A peak)

d)The output capacitance required assuming E_{SR} =0. (3.13µF)

e)The output capacitance required assuming E_{SR} =8mΩ/1000µF. (1000µF)

f)The peak voltage and peak current ratings for the semiconductors. (350V, 5.25A, 141V, 26A)

7. Design a Full Bridge DC-DC converter to meet the following requirements:

Input Voltage, V_S =150Vdc ± 50Vdc

Output Voltage, V_o = 5Vdc with a maximum ripple of 150mV p-p.

Output Current, I_o = 10A minimum, 100A maximum.

Switching frequency is 200kHz.

Determine the following:

a) The transformer turns ratio. (20)

b) The duty cycle during minimum, nominal, and maximum input voltage. (1.0, 0.667, 0.5)

c) The critical inductance. (0.3125µH)

d) The peak input current, using the inductance value determined in part c). (5.5A)

e) The output capacitance assuming no E_{SR} . (41.7µF)

f) The output capacitance assuming capacitors are available in cans of 1000 uF and 15 milliohms E_{SR} in each can. (2000µF)

8. Design a 500Vdc, 10KW power supply for a resistive load using a transformer and four transistors in a Full Bridge configuration. The input voltage varies from 176 to 265 Vdc. The switching frequency must be 50kHz, and the minimum load is 200W. The output ripple is to be 6Vp-p. Determine:

a)The transformer turns ratio, assuming the maximum duty cycle must not exceed 95%. (0.334)

b)The minimum duty cycle. (0.631)

c)The critical inductance. (2.31µH)

d)The output capacitance assuming E_{SR} =0. (166µF)

e)The output capacitance assuming capacitors are available in 100µF cans, each with E_{SR} =1Ω. (100µF)

f)The peak voltage and peak current ratings for the semiconductors. (265V, 61.1A, 1587V, 20.4A)

9. Design a Full Bridge DC-DC converter to meet the following requirements:

Input Voltage, V_S =50Vdc ± 10Vdc

Output Voltage, V_o = 5Vdc with a maximum ripple of 150mV p-p.

Output Current, I_o = 30A minimum, 120A maximum.

Switching frequency is 40kHz.

Determine the following:

a) The transformer turns ratio. (8)

b) The duty cycle during minimum, nominal, and maximum input voltage. (1.0, 0.8, 0.67)

c) The critical inductance. (0.347µH)

d) The output capacitance assuming no E_{SR} . (625µF)

e) The output capacitance assuming capacitors are available in

cans of 1000 µF and 15 milliohms E_{SR} in each can. (6000µF)

f)The peak voltage and peak current ratings for the semiconductors. (60V, 18.75A, 15V, 150A)

7.10.5 Half Bridge Converters

10. Design a Half Bridge Converter to meet the following requirements;

V_S =300±50Vdc,

V_0 =50Vdc,

Maximum ripple=200 mV p-p,

I_0 =1A minimum, 25A maximum,

Switching frequency is 200kHz.

Determine:

a)The transformer turns ration such that the maximum duty cycle does not exceed 99%. (2.475)

b)The minimum duty cycle and under what conditions it occurs. (0.707)

c)The minimum inductance required and the worst case average and peak current rating for this inductor. (18.3µH, 25A average, 26A peak)

d)The output capacitance required assuming E_{SR} =0. (3.13µF)

e)The output capacitance required assuming capacitors are available in 1000µF cans each with E_{SR} =8mΩ. (1000µF)

f)The peak voltage and peak current ratings for the semiconductors. (350V, 10.5A, 141V, 26A)

7.10.6 Push-Pull Converters

11. Design a Push-Pull Converter to meet the following requirements;

V_S =320±50Vdc,

V_0 =50Vdc,

Maximum ripple=150 mV p-p,

I_0 =5A minimum, 50A maximum,

Switching frequency is 120kHz.

Determine:

a)The transformer turns ration such that the maximum duty cycle does not exceed 95%. (5.13)

b)The minimum duty cycle and under what conditions it occurs. (0.69)

c)The minimum inductance required and the worst case average and peak current rating for this inductor. (6.46µH, 50A average, 55A peak)

d)The output capacitance required assuming E_{SR} =0. (34.7µF)

e)The output capacitance required assuming E_{SR} =50mΩ/1000µF. (4,000µF)

f)The peak voltage and peak current ratings for the semiconductors. (740V, 10.7A, 144V, 55A)

12. Design a Push-Pull Converter to meet the following requirements;

V_S =300±50Vdc,

V_0 =50Vdc,

Maximum ripple=200 mV p-p,

I_0 =1A minimum, 25A maximum,

Switching frequency is 200kHz.

Determine:

a)The transformer turns ration such that the maximum duty cycle does not exceed 99%. (4.95)

b)The minimum duty cycle and under what conditions it occurs. (0.707)

c)The minimum inductance required and the worst case average and peak current rating for this inductor. (18.3µH, 25A average, 26A peak)

d)The output capacitance required assuming E_{SR} =0. (3.13µF)

e)The output capacitance required assuming capacitors are available in 1000µF cans, each with E_{SR} =8mΩ. (1000µF)

f)The peak voltage and peak current ratings for the semiconductors. (700V, 5.25A, 141V, 26A)

7.10.7 Flyback Converters

13. Design a Flyback Converter to meet the following requirements;

V_S =320±50Vdc,

V_0 =50Vdc,

Maximum ripple=150 mV p-p,

I_0 =5A minimum, 50A maximum,

Switching frequency is 120kHz.

Determine:

a)The transformer turns ration such that the duty cycle is 50% at nominal input voltage. (6.4)

b)The minimum and maximum duty cycle and under what conditions each occurs. (0.464, 0.533)

c)The minimum inductance required (referred to the primary) and the worst case average and peak current rating for this inductor. (490µF, 9.2A average, 19.56A peak)

d)The output capacitance required assuming E_{SR} =0. (1506µF)

e)The output capacitance required assuming capacitors are available in 1000µF cans each with E_{SR} =50mΩ. (37,000µF)

f)The peak voltage and peak current ratings for the semiconductors. (690V, 19.56A, 107.8V, 125.2A)

14. Design a Flyback Converter to meet the following requirements;

V_S =300±50Vdc,

V_0 =50Vdc,

Maximum ripple=200 mV p-p,

I_0 =1A minimum, 25A maximum,

Switching frequency is 200kHz.

Determine:

a)The transformer turns ration such that the duty cycle is 50% at nominal input voltage. (6)

b)The minimum and maximum duty cycle. (0.462, 0.545)

c)The minimum inductance required (referred to the secondary) and the worst case average and peak current rating for this inductor. (36.2µH, 54.95A average, 56.5A peak)

d)The output capacitance required assuming E_{SR} =0. (340.6µF)

e)The output capacitance required assuming E_{SR} =8mΩ/1000µF. (2000µF)

f)The peak voltage and peak current ratings for the semiconductors. (650V, 9.42A, 108V, 56.5A)

15. Design a flyback converter to meet the following requirements:

Input Voltage, V_S = 300 V

Output Voltage, V_0 = 20 Vdc, maximum ripple of 250 mV p-p

Output Current, I_0 = 1.0 A

Duty cycle = 0.5

Switching frequency = 500 kHz

Determine the following:

a) The transformer turns ratio. (15)

b) The critical transformer magnetizing inductance referred to the primary. (1125µH)

c) The output capacitance assuming no E_{SR} . (4µF)

e) The output capacitance assuming capacitors come in cans of100 µF and 500 milliohms E_{SR} in each can. (800µF)

16. Design a 500Vdc, 100W power supply for a resistive load using Flyback Converter. The input voltage is 312 Vdc ±15%. The switching frequency must be 150kHz, and the minimum load is 20W. The output ripple is 6Vp-p. Determine:

a)The transformer turns ratio, assuming the duty cycle must 50% at nominal input and maximum output. (0.624)

b)The minimum and maximum duty cycle. (0.465, 0.541)

c)The critical magnetizing inductance, referred to the primary. (4.64mH)

d)The output capacitance assuming E_{SR} =0. (120µF)

e)The peak voltage and peak current ratings for the semiconductors. (671V, 0.8A,1075V, 0.5A)

17. Design a Fyback Converter to meet the following requirements;

Output Voltage, V_o =150Vdc,

Output Current, I_o =5A minimum, 50A maximum,

You are given a capacitor of 470µF, and a transformer with a turns ratio of 2:1, a magnetizing inductance of 100 µH on the input side, (25µH on the output side. Determine:

a)The input voltage range for $0.4 < \delta < 0.6$. (200V to 450V)

b)The minimum switching frequency to keep inductor current from going to zero. (216kHz)

c)The minimum switching frequency to keep the output ripple within 75 mV p-p. (851kHz)

d)The peak voltage and peak current ratings for the semiconductors if the switching frequency is 200kHz. (750V, 65.5A, 375V, 131A)