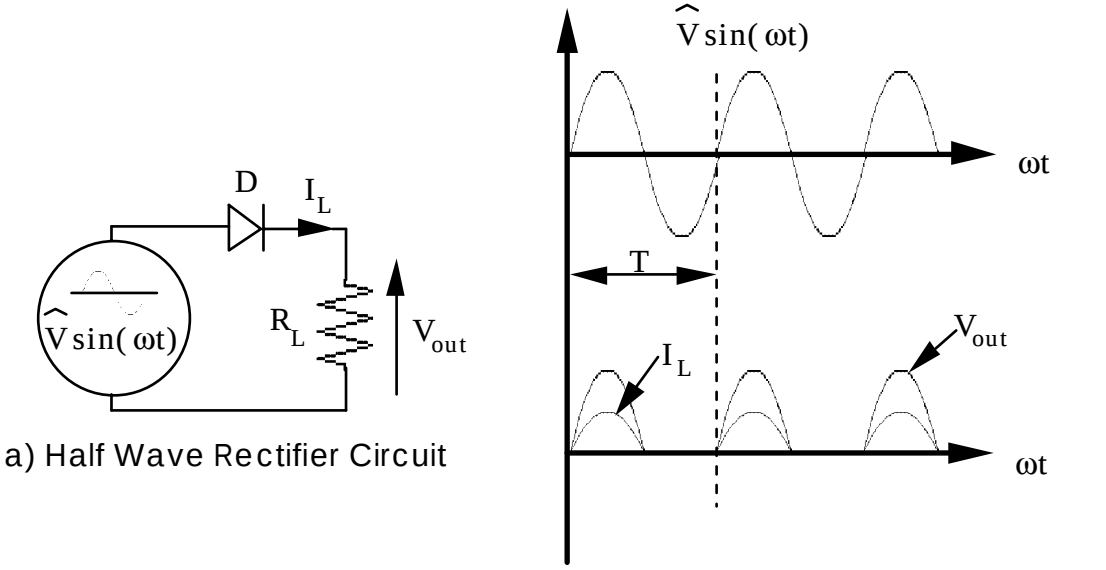
CHAPTER 6
BASIC POWER ELECTRONIC CIRCUITS

6.1 RECTIFIER CIRCUITS

There are two basic types of rectifier circuits as classified by their output waveform: half wave rectifier circuits, and full wave rectifier circuits. Full wave rectifiers may be further classified as to whether they utilize a full bridge or half bridge configuration of diodes. Each of these circuits will be described in this section.

6.1.1 Half Wave Rectifier Circuit

The basic half wave rectifier circuit is shown in **Figure 6.1**



a) Half Wave Rectifier Circuit

b) Voltage and Current Waveforms

Figure 6.1 Basic Half Wave Rectifier Circuit

Diode D conducts, (acts like a short circuit), when the source voltage, $\hat{V}\sin(\omega t)$ is positive. Conversely diode D is reverse biased, (acts like an open circuit), when $\hat{V}\sin(\omega t)$ is negative. Therefore the expression for the output voltage can be determined:

$$V_{out} = \hat{V}\sin(\omega t) \qquad \text{for } 0 < \omega t < \pi$$
$$= 0 \qquad \text{for } \pi < \omega t < 2\pi \text{ etc.}$$

The performance of rectifier circuits is characterized by the following parameters:

a) DC value of the output voltage;

$$V_{dc} = \frac{1}{2\pi}\int_0^{2\pi} V_{out}\partial(\omega t) = \frac{1}{2\pi}\int_0^{\pi} \hat{V}\sin(\omega t)\partial(\omega t) = \frac{\hat{V}}{\pi}$$

$$= 0.318\,\hat{V}$$

b) RMS value of the output voltage;

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} V_{out}^2\partial(\omega t)} = \sqrt{\frac{1}{2\pi}\int_0^{\pi}\left[\hat{V}\sin(\omega t)\right]^2\partial(\omega t)}$$

$$= 0.5\,\hat{V}$$

c) Ripple content, (in rms), of the output voltage;

$$V_{ripple} = \sqrt{V_{rms}^2 - V_{DC}^2}$$
$$= 0.386\,\hat{V}$$

d) Ripple Factor, R.F., of the output voltage;

$$R.F. = \frac{V_{ripple}}{V_{DC}} = \frac{0.386\hat{V}}{0.318\hat{V}} = 1.21$$

Diode ratings (stresses) are;

a) Peak Inverse Voltage, PIV.
PIV occurs across the diode when it is reverse biased and not conducting. In the circuit shown in **Figure 6.1** the diode will be reverse biased during the entire negative half of the source voltage waveform. The peak of the negative waveform occurs at $\omega t = 3\pi/2$ at which time:

$$PIV = -\hat{V}\sin(\omega t) = -\hat{V}\sin(3\pi/2) = \hat{V}$$

b) Peak diode current, $\hat{I}$.
In the circuit of **Figure 6.1** the peak diode current will be the same as the peak of the load current, I_L , because both elements are in series. Therefore;

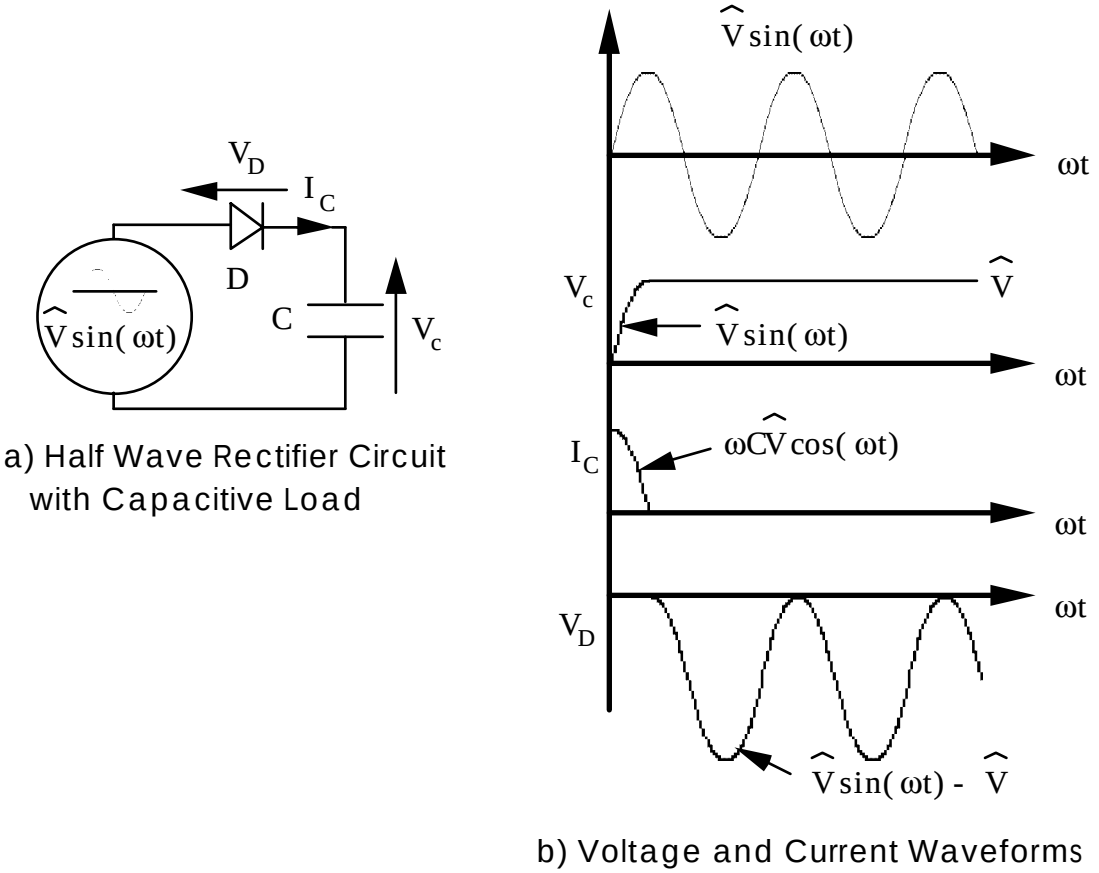
$$\hat{I} = \hat{I}_L = \frac{\hat{V}}{R_L}$$

c) Diode RMS current, I_{rms}.
In the circuit of **Figure 6.1** the rms of the diode current will be the same as the rms of the load current, I_L , because both elements are in series. Therefore;

$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{0.5\hat{V}}{R_L}$$

6.1.2 Half Wave Rectifier Circuit With Capacitive Load (Peak Detector Circuit)

A basic half wave rectifier circuit with capacitive load is shown in **Figure 6.2.**



a) Half Wave Rectifier Circuit with Capacitive Load

b) Voltage and Current Waveforms

Figure 6.2 Half Wave Rectifier Circuit With Capacitive Load

Assume that the initial capacitor voltage, V_C , is zero and that diode D will be forward biased and will conduct during the positive part of the source voltage, when $I_m \sin(\omega t) > 0$. As long as D is conducting,

$$v_c(t) = \hat{V}\sin(\omega t)$$

and,

$$i(t) = C\frac{\partial V}{\partial t} = \omega C\hat{V}\cos(\omega t)$$

Note that diode D will stop conducting when the current, i(t), goes to zero. This occurs at $\omega t = \pi/2$. At this time;

$$v_c(t) = \hat{V}\sin(\pi/2) = \hat{V}$$

The capacitor voltage will remain at this value because the diode is reversed biased and cannot discharge the capacitor. Assuming an ideal capacitor and no load, the capacitor has no way of discharging and will remain at this voltage.

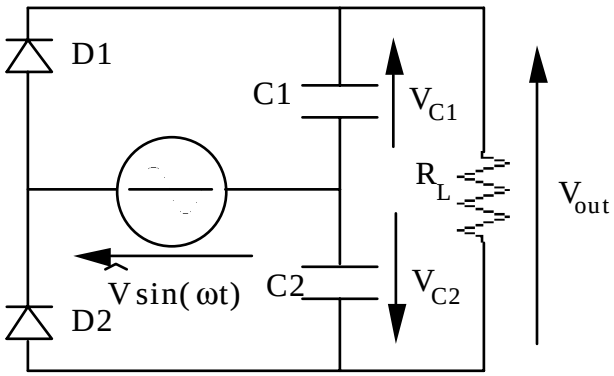
Even at the next positive peak of the source voltage at $\omega t = 5\pi/2$, the diode will still not conduct because the source voltage will still not be greater than the capacitor voltage and there will be no net positive voltage to turn on the diode.

In effect the capacitor remains charged at the positive peak of the input voltage waveform. This is called a Positive Peak Detector.

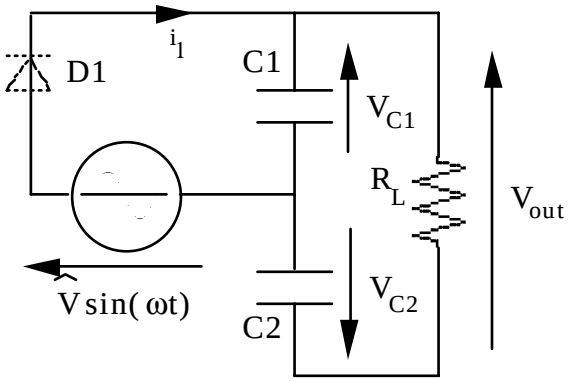
In real circuits with real capacitors that have a self discharge and real loads the capacitor voltage will discharge slightly between cycles and this discharge will be 'topped off' each time the source voltage goes to a positive peak at which time a narrow pulse of current will flow through the diode.

6.1.3 Voltage Doubler

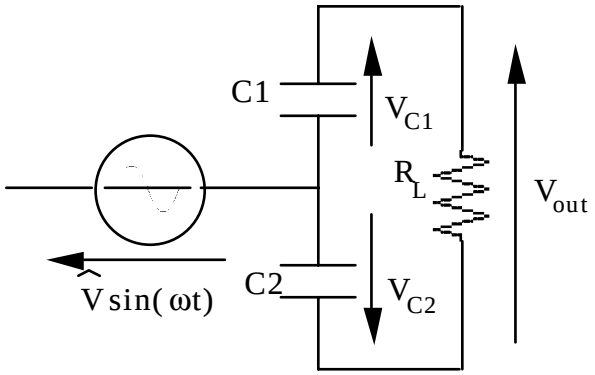
A basic voltage doubler circuit is shown in **Figure 6.3**



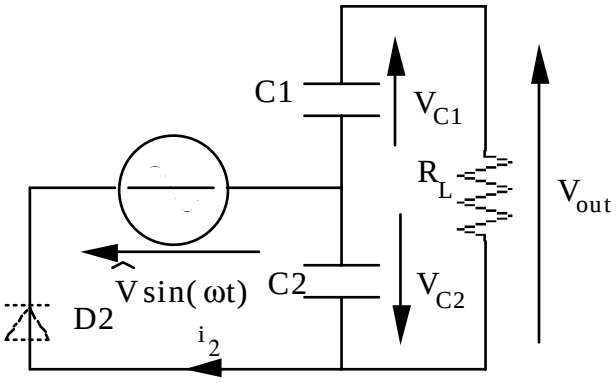
a) Basic Voltage Doubler Circuit



b) Equivalent Circuit When D1 is conduting



c) Equivalent Circuit When Neither Diode is Conducting



d) Equivalent Circuit When D2 is Conducting

Figure 6.3 Basic Voltage Doubler Circuit

This circuit can best be analyzed by first assuming that capacitors C1 and C2 are initially uncharged and then breaking down the total circuit into different equivalent circuits during each polarity (each half cycle) of the voltage source waveform.

The equivalent circuit during the positive half cycle of $\hat{V}\sin(\omega t)$ is shown in **Figure 6.3b.** During this half cycle diode D1 conducts and can be represented by a short circuit, whereas diode D2 is reverse biased and can be represented by an open circuit. Since diode D1 is a short circuit, the voltage, V_{C1} , across capacitor C1 will be:

$$v_{C1}(t) = \hat{V}\sin(\omega t)$$

and,

$$i_1(t) = C\frac{\partial V}{\partial t} = \omega C\hat{V}\cos(\omega t)$$

Note that diode D1 will stop conducting when the current, $i_1(t)$, goes to zero. This occurs at $\omega t = \pi/2$. At this time;

$$v_{C1}(t) = \hat{V}\sin(\pi/2) = \hat{V}$$

The capacitor voltage will remain at this value because diode D1 is reversed biased and cannot discharge the capacitor. Assuming an ideal capacitor and light load, the capacitor will remain at this voltage for the remainder of the cycle.
The above equations are identical to those of the peak detector circuit described in section 6.1.2, and in fact this part of the voltage doubler circuit is a positive peak detector.

Equivalent circuit for remainder of the positive half cycle of $\hat{V}\sin(\omega t)$ is shown in **Figure 6.3c.** During this time C1 stays charged at $\hat{V}$, except for slight discharge through the load resistor R_L, which can be ignored for a first approximation.

The equivalent circuit during the negative half cycle of $\hat{V}\sin(\omega t)$ is shown in **Figure 6.3d.** During this half cycle diode D2 conducts and can be represented by a short circuit, whereas diode D1 is now reverse biased and it can be represented by an open circuit. Since diode D2 is a short circuit, the voltage, V_{C2}, across capacitor C2 will be:

$$v_{C2}(t) = \hat{V}\sin(\omega t)$$

and,

$$i_2(t) = C\frac{\partial V}{\partial t} = \omega C\hat{V}\cos(\omega t)$$

Note that diode D2 will stop conducting when the current, $i_2(t)$, goes to zero. This occurs at $\omega t = 3\pi/2$. At this time;

$$v_{C2}(t) = \hat{V}\sin(3\pi/2) = -\hat{V}$$

The capacitor voltage will remain at this value because diode D2 is reversed biased and cannot discharge the capacitor. Assuming an ideal capacitor and light load, the capacitor will remain at this voltage for the remainder of the cycle.
The above equations are similar but opposite polarity to those of the peak detector circuit described in section 6.1.2, and in fact this part of the voltage doubler circuit is a *negative* peak detector.

Equivalent circuit for the remainder of the negative half cycle of $\hat{V}\sin(\omega t)$ is the same as for the remainder of the positive half cycle shown in **Figure 6.3c.** During this time C2 stays charged at $-\hat{V}$, except for slight discharge through the load resistor R_L, which can be ignored for a first approximation.
Throughout the above analysis the output voltage $\hat{V}$ can be determined by;

$$\hat{V} = - v_{C2} + v_{C1}$$

Substitute for;

$$v_{C1} = \hat{V}$$
$$v_{C2} = -\hat{V}$$

and obtain;

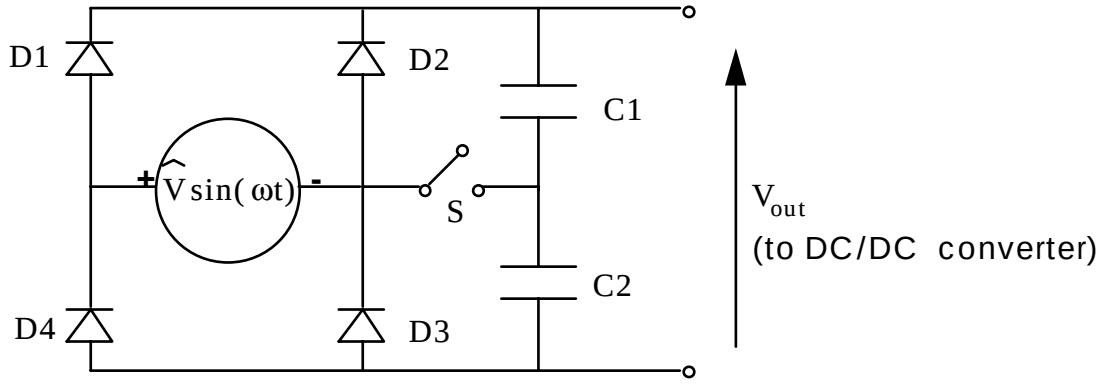
$$V_{out} = - (-\hat{V}) + \hat{V} = 2\hat{V}$$ double the input voltage peak.

This circuit only works for relatively light loading, such that the discharge through the load is negligible compared to the peak voltage. In general the discharge RC time constant should be larger than the discharge time available, $2\pi/\omega$;

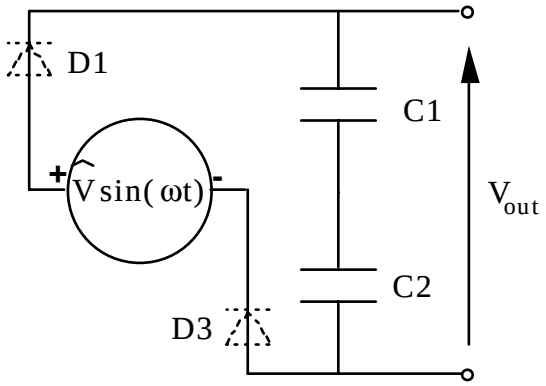
$$R_L C > \frac{2\pi}{\omega}$$

Example problem 6-1

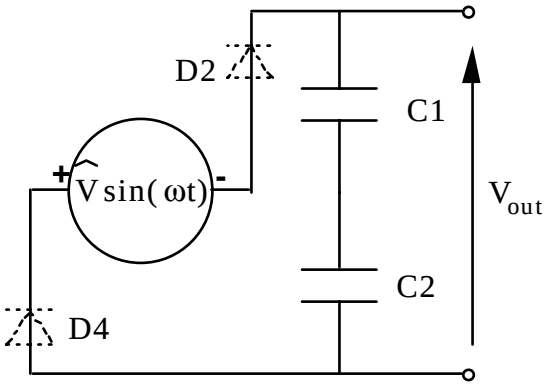
The circuit in **Figure 6.4** shows the input stage to an AC/DC power supply. The input voltage, V_{in} can be either 110 Vac rms or 220 Vac rms.
However, it is important to maintain V_{out} approximately the same regardless of whether V_{in} is 110 or 220 Vac.
Determine what position switch S should be in, if V_{in} is 110Vac and if V_{in} is 220Vac to maintain constant V_{out}.



a) Input Stage Circuit

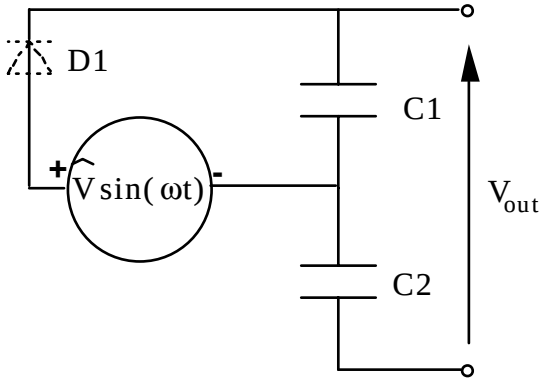


During positive half cycle

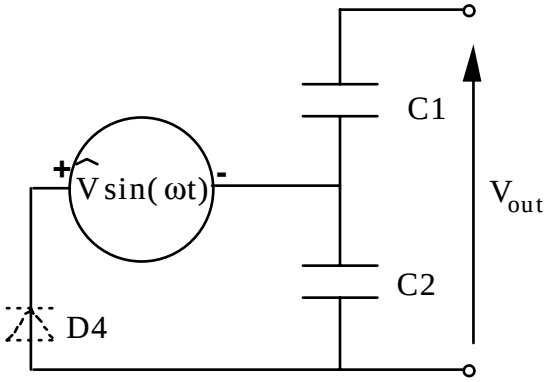


During negative cycle

b) Equivalent Circuits With Switch Open



During positive half cycle



During negative half cycle

c) Equivalent Circuits With Switch Closed

Figure 6.4 Input Stage For An AC/DC Power Supply

Solution to example 6-1

a) With switch S in the open position. The equivalent circuit is shown in **Figure 6.4b**
When V_{in} is positive, diodes D1 and D3 will conduct and charge up capacitors C1 and C2 in series to the peak of V_{in};

$$V_{C1} + V_{C2} = \hat{V}$$

also

$$V_{out} = V_{C1} + V_{C2} = \hat{V}$$

Similarly, when V_{in} is negative, diodes D2 and D4 will conduct and charge up capacitors C1 and C2 in series to the peak of V_{in}, and again

$$V_{out} = V_{C1} + V_{C2} = \hat{V}$$

Thus with switch S in the open position V_{out} will be equal to $\hat{V}$.

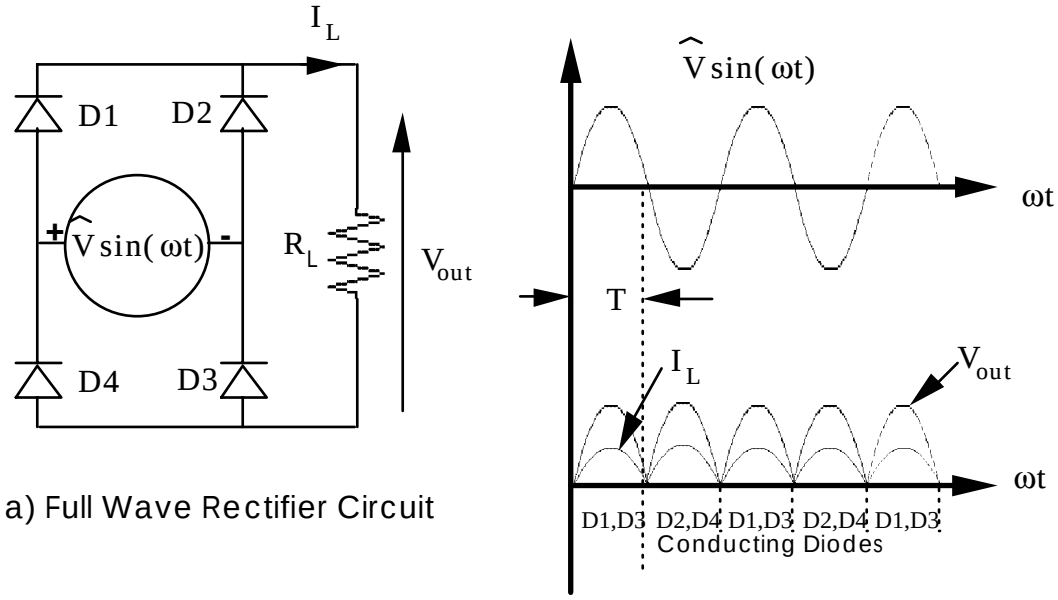
b) With switch S closed, the equivalent circuit is shown in **Figure 6.4c**
This is our basic voltage doubler circuit with diodes D2, D3 across C1, C2.
However, in a voltage doubler circuit capacitors C1, C2 are always positively charged (due to diodes D1, D4) such that D2, D3 are reverse biased. Therefore, because D2, D3 are reverse biased they are open circuit and can be ignored. Therefore for the switch closed the circuit becomes a voltage doubler and for a voltage doubler;

$$V_{out} = 2\hat{V}.$$

In summary, with S open the output voltage will be $\hat{V}$, and with S closed the output voltage will be $2\hat{V}$. Therefore the output voltage can be kept constant by setting S open when V_{in} is 220 Vac, ($V_{out} = \hat{V} = \sqrt{2} \times 220 = 311$Vdc), and setting S closed when V_{in} is 110 Vac, ($V_{out} = 2\hat{V} = 2\sqrt{2} \times 110 = 311$Vdc).

6.1.4 Full Wave Rectifier Circuit Using a Full Bridge Configuration

A basic full wave rectifier circuit is shown in **Figure 6.5.** This circuit utilizes four diodes in an 'H" configuration, which is also known as a 'full bridge configuration'.



a) Full Wave Rectifier Circuit

b) Voltage and Current Waveforms

Figure 6.5 Basic Full Wave Rectifier Circuit

Diodes D1, D3 conduct when $\hat{V}\sin(\omega t)$ is positive at which time the circuit behaves exactly like the half wave rectifier circuit described in section 6.1.1. When $\hat{V}\sin(\omega t)$ is negative diodes D2, D4 conduct and the circuit behaves again exactly like the half wave rectifier circuit described in secion 6.1.1. Thus a full wave rectifier circuit behaves a lot like two half wave rectifiers superimposed on each other.

The performance parameters for a full wave rectifier circuit can be determined:

a) DC value of the output voltage;

$$V_{dc} = \frac{1}{2\pi}\int_0^{2\pi} V_{out}\,\partial(\omega t) = \frac{1}{\pi}\int_0^{\pi} \hat{V}\sin(\omega t)\,\partial(\omega t) = \frac{2\hat{V}}{\pi}$$

$$= 0.637\,\hat{V} = 0.9\,V_{rms}$$

b) RMS value of the output voltage;

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} V_{out}^2\,\partial(\omega t)} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\hat{V}\sin(\omega t)\right]^2\partial(\omega t)}$$

$$V_{rms} = \frac{\hat{V}}{\sqrt{2}}$$

c) Ripple content, (in rms), of the output voltage;

$$V_{ripple} = \sqrt{V_{rms}^2 - V_{DC}^2}$$
$$= 0.308\,\hat{V}$$

d) Ripple Factor, R.F., of the output voltage;

$$R.F. = \frac{V_{ripple}}{V_{DC}} = \frac{0.308\hat{V}}{0.637\hat{V}} = 0.483$$

Diode ratings (stresses) are;

a) Peak Inverse Voltage, PIV.
PIV occurs across each diode when it is reverse biased and not conducting. In the circuit shown in **Figure 6.5** diodes D2, D4 will be reverse biased during the entire positive half of the source voltage waveform when diodes D1, D3 are conducting. The peak of the positive waveform occurs at $\omega t = \pi/2$ at which time:

$$PIV = -\hat{V}\sin(\omega t) = -\hat{V}\sin(\pi/2) = \hat{V}$$

Similarly diodes D1, D3 will be reverse biased during the entire negative half cycle when diodes D2, D4 are conducting. PIV for these diodes will occur at $\omega t = 3\pi/2$ at which time:

$$PIV = \hat{V}\sin(\omega t) = \hat{V}\sin(3\pi/2) = -\hat{V}$$

b) Peak diode current, $\hat{I}$.
In the circuit of **Figure 6.5** the peak current through each diode will be the same as the peak of the load current, I_L, because each diode is in series with the load during its conduction interval. Therefore;

$$\hat{I} = \frac{\hat{V}}{R_L}$$

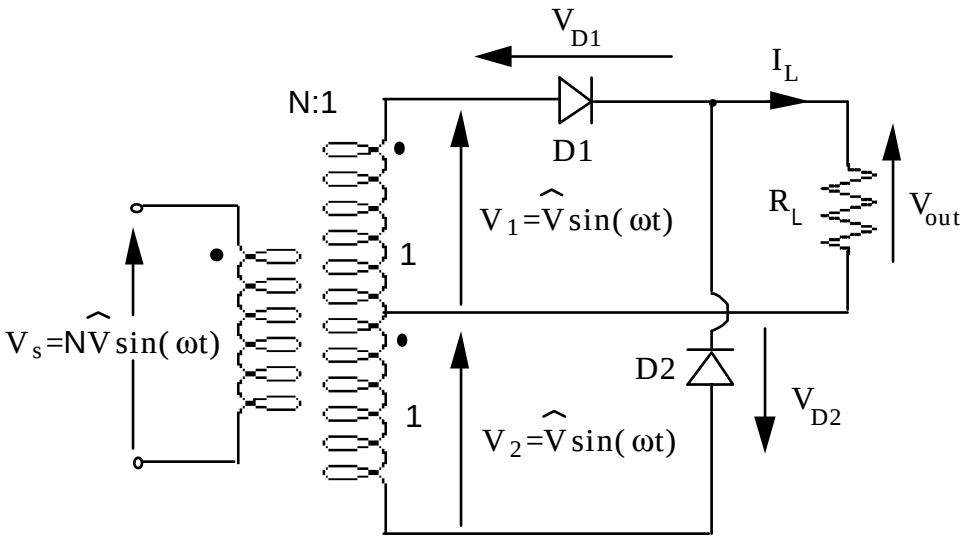
c) Diode RMS current, I_{rms}.
In the circuit of **Figure 6.5** the rms current of each diode will be the same as the rms of *half* the load current waveform, because each diode conducts the load current for only half of each cycle. Therefore;

$$I_{rms} = \frac{V_{rms}}{\sqrt{2}R_L} = \frac{\hat{V}}{2R_L}$$

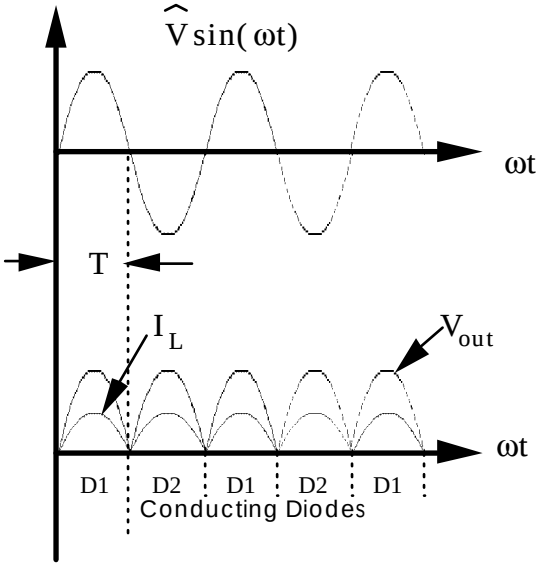
Note that four diodes are required for a full bridge circuit but each pair of diodes only conducts for half the time. Also there are two diodes in series with the load during each half cycle, thus there will be double the V_f drop in this circuit and hence double the power losses.

6.1.5 Full Wave Rectifier Circuit Using a Half Bridge Configuration

Another full wave rectifier circuit is shown in **Figure 6.6.** This circuit utilizes two diodes in a configuration that is known as a 'half bridge'. This circuit also requires a centre-tapped transformer and is therefore also known as a 'centre-tapped rectifier' configuration.



a) Basic Circuit



b) Voltage and Current Waveforms

Figure 6.6 Half Bridge (Center Tapped) Rectifier Circuit

Diode D1 conducts when $\hat{V}\sin(\omega t)$ is positive at which time diode D2 is reverse biased and open circuit. The circuit then behaves exactly like the half wave rectifier circuit

described in section 6.1.1. When $\hat{V}\sin(\omega t)$ is negative diode D2 conducts and diode D1 is now reverse biased and becomes an open circuit. The circuit now behaves again exactly like the half wave rectifier circuit described in secion 6.1.1. Thus this half bridge (center-tapped) rectifier circuit also behaves a lot like two half wave rectifiers superimposed on each other.

The performance parameters for half bridge rectifier circuit are identical to those of the full bridge rectifier described in section 6.1.4:

a) DC value of the output voltage;

$$V_{dc} = \frac{1}{2\pi}\int_0^{2\pi} V_{out}\,\partial(\omega t) = \frac{1}{\pi}\int_0^{\pi} \hat{V}\sin(\omega t)\,\partial(\omega t) = \frac{2\hat{V}}{\pi}$$

$$= 0.637\,\hat{V} = 0.9\,V_{rms}$$

b) RMS value of the output voltage;

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} V_{out}^2\,\partial(\omega t)} = \sqrt{\frac{1}{\pi}\int_0^{\pi} \left[\hat{V}\sin(\omega t)\right]^2\,\partial(\omega t)}$$

$$= \frac{\hat{V}}{\sqrt{2}}$$

c) Ripple content, (in rms), of the output voltage;

$$V_{ripple} = \sqrt{V_{rms}^2 - V_{DC}^2}$$

$$= 0.308\,\hat{V}$$

d) Ripple Factor, R.F., of the output voltage;

$$R.F. = \frac{V_{ripple}}{V_{DC}} = \frac{0.308\hat{V}}{0.637\hat{V}} = 0.483$$

Diode ratings (stresses) are somewhat different than those for the full wave rectifier circuits:

a) Peak Inverse Voltage, PIV.
PIV occurs across each diode when it is reverse biased and not conducting. In the circuit shown in **Figure 6.6** diode D2 will be reverse biased during the entire positive half of the source voltage waveform when diode D1 is conducting. During this interval the voltage across D2 will be;

$$V_{D2} = -V_1 - V_2 = -\hat{V}\sin(\omega t) - \hat{V}\sin(\omega t) = -2\hat{V}\sin(\omega t)$$

The negative peak of this waveform occurs at $\omega t = \pi/2$ at which time:

$$PIV = -2\hat{V}\sin(\omega t) = -2\hat{V}\sin(\pi/2) = -2\hat{V}$$

Similarly diode D1 will be reverse biased during the entire negative half cycle when diode D2 is conducting. PIV for D1 will occur at $\omega t = 3\pi/2$ at which time:

$$PIV = 2\hat{V}\sin(\omega t) = 2\hat{V}\sin(3\pi/2) = -2\hat{V}$$

b) Peak diode current, $\hat{I}$.
In the circuit of **Figure 6.6** the peak current through each diode will be the same as the peak of the load current, I_L, because each diode is in series with the load during its conduction interval. Therefore;

$$\hat{I} = \frac{\hat{V}}{R_L}$$

c) Diode RMS current, I_{rms}.
In the circuit of **Figure 6.6** the rms current of each diode will be the same as the rms equivalent of *half* the load current waveform, because each diode conducts the load current for only half of each cycle. Therefore;

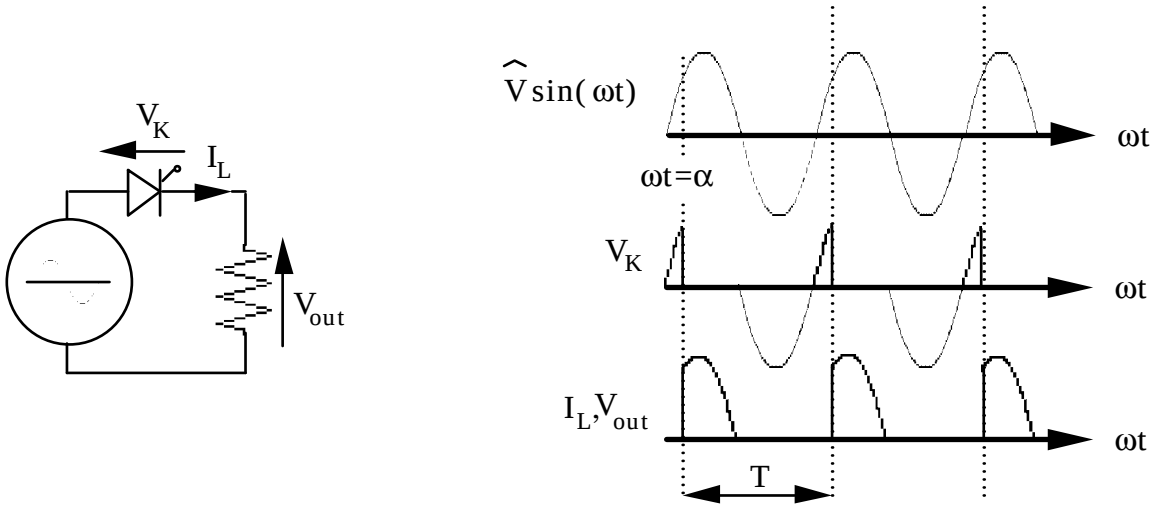
$$I_{rms} = \frac{V_{rms}}{\sqrt{2}R_L} = \frac{\hat{V}}{2R_L}$$

Note that two diodes are required for a half bridge (center-tapped) circuit but each diode only conducts for half the time. Only one diode is in series with the load during each half cycle, thus there will be only one V_f drop in this circuit. Also in a half bridge (centre-tapped) circuit each diode has double the PIV as for a full bridge circuit. Thus half bridge (centre-tapped) configurations are preferred for low voltage applications where V_f drops are significant but PIV isn't, such as a 5V output power supply.
However, a centre-tapped transformer is also required for this circuit. Thus centre-tapped configurations are preferred when a transformer is already required for some other reason such as voltage step-down or isolation.

6.2 PHASE CONTROLLED RECTIFIER CIRCUITS

6.2.1 Half Wave Phase Controlled Rectifier

A basic half wave phase controlled rectifier circuit is shown in **Figure 6.7**



a) Half Wave Phase Control Circuit b) voltage and current waveforms

Figure 6.7 Basic Half Wave Phase Controlled Rectifier Circuit

This circuit is very similar to the half wave rectifier circuit described in section 6.1 The major difference is that an SCR is used instead of a diode and thus the SCR can be turned on at any point in the positive half cycle of $\hat{V}\sin(\omega t)$. The point at which the SCR is turned on is called the firing angle. The various waveforms in this circuit are shown in **Figure 6.7** for an arbitrary firing angle of α. It can be seen that the dc component of the output, V_{out}, can be controlled by controlling the firing angle, α.

The performance parameters for half wave phase controlled rectifier can be determined as follows:

a) DC value of the output voltage;

$$V_{dc} = \frac{1}{2\pi}\int_0^{2\pi} V_{out}\partial(\omega t) = \frac{1}{2\pi}\int_\alpha^{\pi} \hat{V}\sin(\omega t)\partial(\omega t)$$

$$= \frac{\hat{V}}{2\pi}\left[1+\cos(\alpha)\right]$$

b) RMS value of the output voltage;

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_{\alpha}^{2\pi} V_{out}^2 \partial(\omega t)} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi} \left[\hat{V}\sin(\omega t)\right]^2 \partial(\omega t)}$$

$$= \frac{\hat{V}}{2}\left[1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi}\right]^{1/2}$$

c) The expressions for the rms ripple content and the Ripple Factor, (R.F.) of the output voltage are the same as in sections 6.1.1, 6.1.5 and 6.1.6;

$$V_{ripple} = \sqrt{V_{rms}^2 - V_{DC}^2}$$

$$R.F. = \frac{V_{ripple}}{V_{DC}}$$

However, in the case of SCR phase control, these expressions do not simplify.

SCR ratings (Stresses) are;

a) Peak Inverse Voltage, PIV.
PIV occurs across the SCR when it is reverse biased and not conducting. In the circuit shown in **Figure 6.7** the SCR will be reverse biased during the entire negative half of the source voltage waveform. The peak of the negative waveform occurs at $\omega t = 3\pi/2$ at which time:

$$PIV = -\hat{V}\sin(\omega t) = -\hat{V}\sin(3\pi/2) = \hat{V}$$

b) Peak SCR current, $\hat{I}$.
In the circuit of **Figure 6.7** the peak SCR current will be the same as the peak of the load current, I_L, because both elements are in series. Therefore;

$$\hat{I} = \frac{\hat{V}}{R_L}$$

c) SCR RMS current, I_{rms}.
In the circuit of **Figure 6.7** the rms of the SCR current will be the same as the rms of the load current, I_L, because both elements are in series during the entire conduction interval. Therefore;

$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{\hat{V}}{2R_L}\left[1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi}\right]^{1/2}$$

d) Available turn off time, t_q .

In the circuit of **Figure 6.7** the SCR will be reverse biased during the entire negative half cycle of $\hat{V}\sin(\omega t)$, therefore;

$$t_q = \pi/\omega$$

6.2.2 Full Wave Phase Controlled Rectifier

A basic full wave phase controlled rectifier circuit is shown in **Figure 6.8**

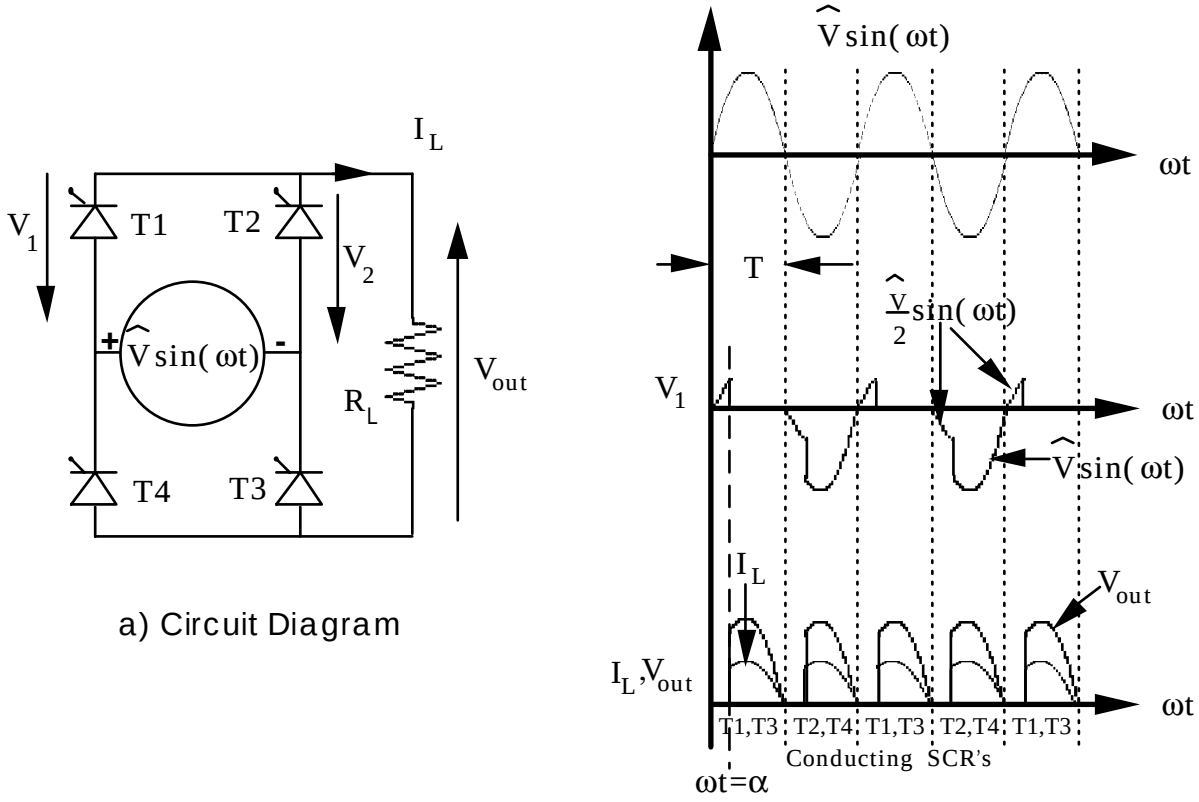


Figure 6.8 Basic Full Wave Phase Controlled Rectifier Circuit

This circuit is very similar to the full wave rectifier circuit described in section 6.5 Again the major difference is that SCR's are used instead of diodes and thus the SCR's can be turned on at any point when it's voltage is positive. The SCR's are turned on in pairs with T1, T3 turned on during the positive half cycle of $V_{\alpha}\sin(\omega t)$, and T2, T4 turned on during the negative half cycle of $\hat{V}\sin(\omega t)$. The various waveforms in this circuit are shown in **Figure 6.8** for an arbitrary firing angle of α. It can be seen that the dc component of the output, V_{out}, can be controlled by controlling the firing angle, α.

The performance parameters for a full wave phase controlled rectifier can be determined as follows:

a) DC value of the output voltage;

$$V_{dc} = \frac{1}{\pi}\int_{\alpha}^{\pi} V_{out}\partial(\omega t) = \frac{1}{\pi}\int_{\alpha}^{\pi} \hat{V}\sin(\omega t)\partial(\omega t)$$

$$= \frac{\hat{V}}{\pi}\left[1+\cos(\alpha)\right]$$

b) RMS value of the output voltage;

$$V_{rms} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi} V_{out}^2 \partial(\omega t)} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi}\left[\hat{V}\sin(\omega t)\right]^2 \partial(\omega t)}$$

$$= \frac{\hat{V}}{2}\left[2-\frac{2\alpha}{\pi}+\frac{\sin(2\alpha)}{\pi}\right]^{1/2}$$

c) The expressions for the rms ripple content and the Ripple Factor, (R.F.) of the output voltage are the same as in sections 6.1.1, 6.1.5 and 6.1.6;

$$V_{ripple} = \sqrt{V_{rms}^2 - V_{DC}^2}$$

$$R.F. = \frac{V_{ripple}}{V_{DC}}$$

However, in the case of SCR phase control, these expressions do not simplify.

SCR ratings (Stresses) are;

a) Peak Inverse Voltage, PIV.
PIV occurs across each SCR when it is reverse biased and not conducting. In the circuit shown in **Figure 6.8** SCR's T2, T4 will be reverse biased during the entire positive half of the source voltage waveform when SCR's T1, T3 are conducting. The peak of the positive waveform occurs at $\omega t = \pi/2$ at which time:

$$PIV = \hat{V}\sin(\omega t) = \hat{V}\sin(\pi/2) = \hat{V}$$

Similarly SCR's T1, T3 will be reverse biased during the entire negative half cycle when SCR's T2, T4 are conducting. PIV for these SCR's will occur at $\omega t = 3\pi/2$ at which time:

$$PIV = -\hat{V}\sin(\omega t) = -\hat{V}\sin(3\pi/2) = \hat{V}$$

b) Peak current, $\hat{I}$.
In the circuit of **Figure 6.8** the peak current through each SCR will be the same as the peak of the load current, I_L , because each SCR is in series with the load during its conduction interval. Therefore;

$$\hat{I} = \frac{\hat{V}}{R_L}$$

c) SCR RMS current, I_{rms}.

In the circuit of **Figure 6.8** the rms current of each SCR will be the same as the rms of *half* the load current waveform, because each SCR conducts the load current for only half of each cycle. Therefore;

$$I_{rms} = \frac{V_{rms}}{\sqrt{2}R_L} = \frac{\hat{V}}{2\sqrt{2}R_L}\left[2 - \frac{2\alpha}{\pi} + \frac{\sin(2\alpha)}{\pi}\right]^{1/2}$$

d) Available turn off time, t_q .

In the circuit of **Figure 6.8** the SCR will be reverse biased during the entire negative half cycle of $\hat{V}\sin(\omega t)$, therefore;

$$t_q = \pi/\omega$$

Note that four SCR's are required for a full bridge circuit but each pair of SCR's only conducts for half the time. Also there are two SCR's in series with the load during each half cycle, thus there will be double the V_f drop in this circuit.

6.2.3 Full Wave Phase Controlled Rectifier Circuit Using a Half Bridge Configuration

Another full wave phase controlled rectifier circuit is shown in **Figure 6.9.** Like the similar rectifier circuit described in section 6.1.6 this circuit utilizes a 'half bridge' configuration that consists of two SCR's. This circuit also requires a centre-tapped transformer and is therefore also known as a 'centre-tapped phase controlled rectifier' configuration.

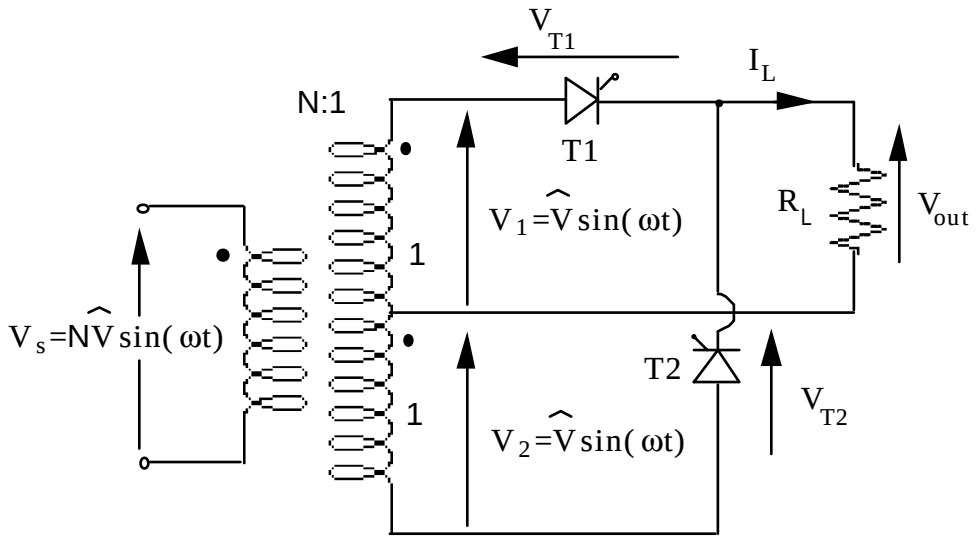


Figure 6.9 Half Bridge (Center Tapped) Phase Controlled Rectifier

SCR T1 conducts when $\hat{V}\sin(\omega t)$ is positive at which time SCR T2 is reverse biased and open circuit. The circuit then behaves exactly like the half wave phase controlled rectifier circuit described in section 6.2.1. When $\hat{V}\sin(\omega t)$ is negative SCR T2 conducts and SCR T1 is now reverse biased and becomes an open circuit. The circuit now behaves again exactly like the half wave phase controlled rectifier circuit described in secion 6.2.1. Thus this half bridge (center-tapped) phase controlled rectifier circuit also behaves a lot like two half wave phase controlled rectifiers superimposed on each other.

The performance parameters for half bridge phase controlled rectifier circuit are identical to those of the full wave phase controlled rectifier described in section 6.2.2:

a) DC value of the output voltage;

$$V_{dc} = \frac{1}{\pi}\int_{\alpha}^{\pi} V_{out}\partial(\omega t) = \frac{1}{\pi}\int_{\alpha}^{\pi} \hat{V}\sin(\omega t)\partial(\omega t)$$

$$= \frac{\hat{V}}{\pi}\left[1+\cos(\alpha)\right]$$

b) RMS value of the output voltage;

$$V_{rms} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi} V_{out}^2 \partial(\omega t)} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi}\left[\hat{V}\sin(\omega t)\right]^2 \partial(\omega t)}$$

$$= \frac{\hat{V}}{2}\left[2 - \frac{2\alpha}{\pi} + \frac{\sin(2\alpha)}{\pi}\right]^{1/2}$$

c) The expressions for the rms ripple content and the Ripple Factor, (R.F.) of the output voltage are the same as in sections 6.1.1, 6.1.5 and 6.1.6;

$$V_{ripple} = \sqrt{V_{rms}^2 - V_{DC}^2}$$

$$R.F. = \frac{V_{ripple}}{V_{DC}}$$

However, in the case of SCR phase control, these expressions do not simplify.

SCR ratings (stresses) are somewhat different than those for the full wave phase controlled rectifier circuits, but more similar to those of the half bridge (centre-tapped) diode circuit:

a) Peak Inverse Voltage, PIV.
PIV occurs across each SCR when it is reverse biased and not conducting. In the circuit shown in **Figure 6.9** SCR T2 will be reverse biased during the entire positive half of the source voltage waveform when SCR T1 is conducting. During this interval the voltage across T2 will be;

$$V_{T2} = V_2 + V_1 = \hat{V}\sin(\omega t) + \hat{V}\sin(\omega t) = 2\hat{V}\sin(\omega t)$$

The peak of this waveform occurs at $\omega t = \pi/2$ at which time:

$$PIV = 2\hat{V}\sin(\omega t) = 2\hat{V}\sin(\pi/2) = 2\hat{V}$$

Similarly SCR T1 will be reverse biased during the entire negative half cycle when SCR T2 is conducting. PIV for T1 will occur at $\omega t = 3\pi/2$ at which time:

$$PIV = -2\hat{V}\sin(\omega t) = -2\hat{V}\sin(3\pi/2) = 2\hat{V}$$

b) Peak SCR current, $\hat{I}$.
In the circuit of **Figure 6.9** the peak current through each SCR will be the same as the peak of the load current, I_L, because each SCR is in series with the load during its conduction interval. Therefore;

$$\hat{I} = \frac{\hat{V}}{R_L}$$

c) SCR RMS current, I_{rms}.

In the circuit of **Figure 6.9** the rms current of each SCR will be the same as the rms equivalent of *half* the load current waveform, because each diode conducts the load current for only half of each cycle. Therefore;

$$I_{rms} = \frac{V_{rms}}{\sqrt{2}R_L} = \frac{\hat{V}}{2\sqrt{2}R_L}\left[2 - \frac{2\alpha}{\pi} + \frac{\sin(2\alpha)}{\pi}\right]^{1/2}$$

d) Available turn off time, t_q .

In the circuit of **Figure 6.9** the SCR will be reverse biased during the entire negative half cycle of $\hat{V}\sin(\omega t)$, therefore;

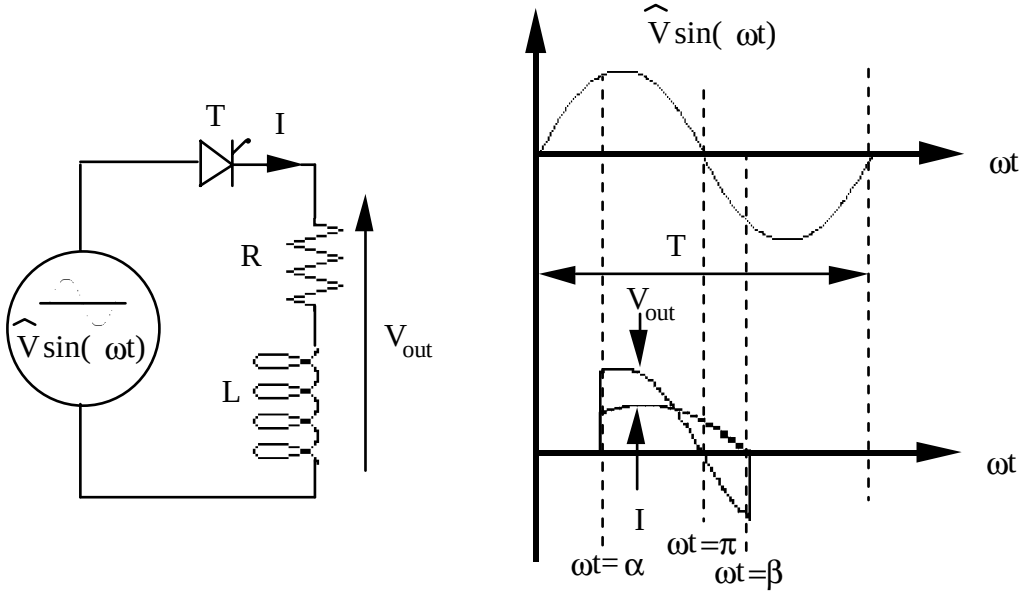
$$t_q = \pi/\omega$$

Note that two SCR's are required for a half bridge (center-tapped) circuit but each SCR only conducts for half the time. Only one SCR is in series with the load during each half cycle, thus there will be only one V_f drop in this circuit. Also in a half bridge (centre-tapped) circuit each diode has double the PIV as for a full bridge circuit. Thus half bridge (centre-tapped) configurations are preferred for low voltage applications where V_f drops are significant but PIV isn't, such as a low voltage power supply.

However, a centre-tapped transformer is also required for this circuit. Thus centre-tapped configurations are preferred when a transformer is already required for some other reason such as voltage step-down or isolation.

6.2.4 Phase Controlled Rectifiers With Inductive Loads

In all the circuits of sections 6.2.1 through 6.2.3 it was assumed that the load was purely resistive. However, in most practical applications the load will have some inductance. The effect of the inductance is to extend the point at which the current goes to zero, (the extinquish angle β), past the point at which the voltage goes to zero, ωt=2π, as shown in **Figure 6.10.**



a) Half Wave Rectifier Circuit b) Voltage and Current Waveforms

Figure 6.10 Phase Controlled Rectifiers With Inductive Loads

The expressions for the output performance parameters, such as V_{dc} and V_{ripple}, get more complex because each integral in the expression now has to be integrated between ωt = α, and ωt = β. Also it is often difficult to determine β. The expressions for the SCR PIV are unchanged but those for peak and rms current become complex because of the complex relationship between voltage and current for inductive loads under phase control.

6.2.5 Phase Controlled Rectifiers With Constant Current Loads

In the extreme case, a highly inductive load can be represented by a constant current source, as shown in **Figure 6.11**. This representation is a very good approximation for loads such as dc motors and field excitation circuits for synchronous machines.

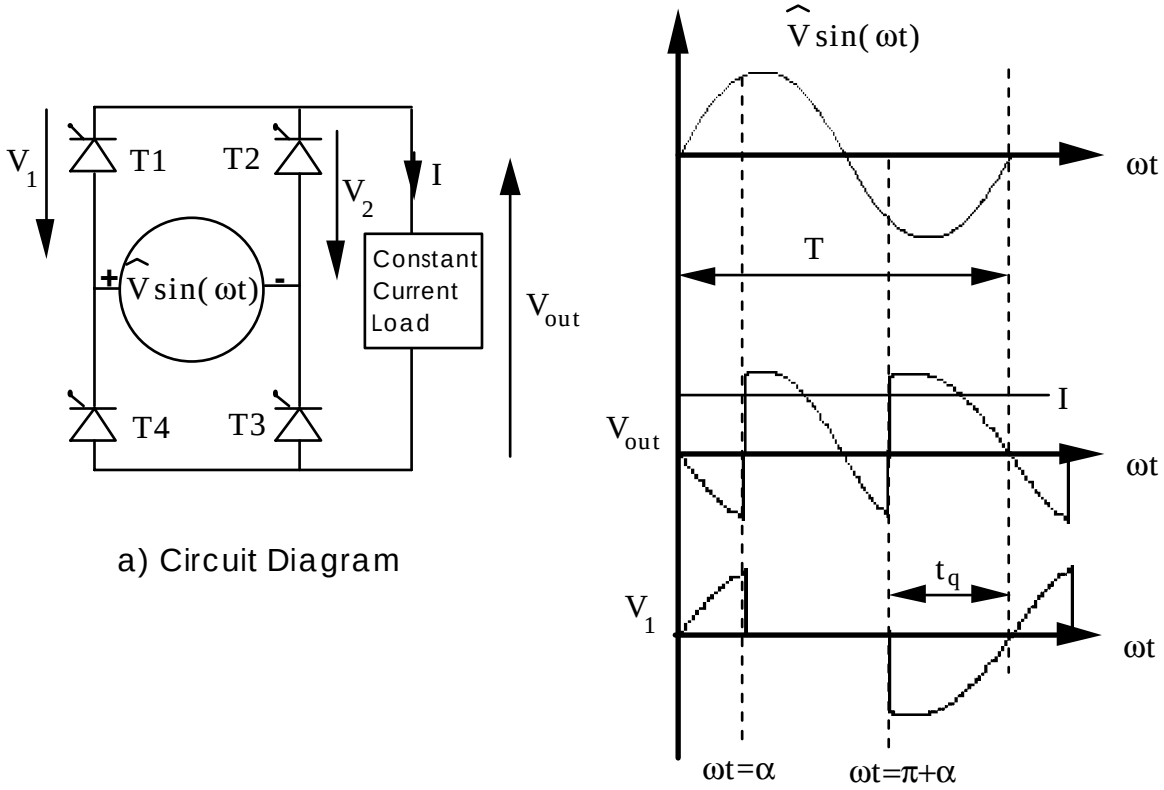


Figure 6.11 SCR Phase Controlled Rectifier With Constant Current Load

The major difference between a constant current load and the resistive load analyzed in sections 6.2.2 and 6.2.3 is that the load current does not go to zero. Therefore each SCR does not turn off until its complementry SCR is fired at the next half cycle. Thus each SCR always conducts for a full half cycle, from $\omega t = \alpha$ to $\omega t = \pi + \alpha$.

The performance parameters for a full wave phase controlled rectifier with constant current load can be determined as follows:

a) DC value of the output voltage;

$$V_{DC} = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_{out}\,\partial(\omega t) = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} \hat{V}\sin(\omega t)\,\partial(\omega t)$$

$$= \frac{2\hat{V}}{\pi}\cos(\alpha) \quad V_{dc}$$

b) RMS value of the output voltage;

$$V_{ripple} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_{out}^2 \partial(\omega t)} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} \left[\hat{V}\sin(\omega t)\right]^2 \partial(\omega t)}$$

$$= \frac{\hat{V}}{\sqrt{2}}$$

It is important to note that the above expression for I_{rms} can be positive or negative, depending on the firing angle, α. The output current, however can only be positive because none of the SCR's can conduct negative current. Nevertheless, with a constant current load, a phase controlled rectifier can produce a negative output voltage, for $\pi/2 < \alpha < \pi$. This means that with a constant current load a phase controlled rectifier can regenerate power from the load.

c) Ripple content, (in rms), of the output voltage;

$$V_{ripple} = \sqrt{V_{rms}^2 - V_{DC}^2} = \sqrt{\left[\frac{\hat{V}}{\sqrt{2}}\right]^2 - \left[\frac{2\hat{V}}{\pi}\cos(\alpha)\right]^2}$$

$$= \hat{V}\sqrt{\frac{\pi^2 - 8\cos^2(\alpha)}{2\pi^2}}$$

d) Ripple Factor, R.F., of the output voltage;

$$R.F. = \frac{V_{ripple}}{V_{DC}} = \hat{V}\sqrt{\frac{\pi^2}{8\cos^2(\alpha)} - 1}$$

SCR ratings (stresses) for constant current loads are similar to those for resistive loads except for the turn off time.

a) Peak Inverse Voltage, PIV.
PIV occurs across each SCR when it is reverse biased and not conducting. In the circuit shown in **Figure 6.11** SCR T2 will be reverse biased during the part of the positive half of the source voltage waveform when SCR T1 is conducting. During this interval the voltage across T2 will be;

$$V_{T2} = V_1 = \hat{V}\sin(\omega t) = \hat{V}\sin(\omega t)$$

The peak of this waveform occurs at $\omega t = \pi/2$ at which time:

$$PIV = \hat{V}\sin(\omega t) = \hat{V}\sin(\pi/2) = \hat{V}$$

Similarly SCR T1 will be reverse biased during the entire negative half cycle when SCR T2 is conducting. PIV for T1 will occur at $\omega t = 3\pi/2$ at which time:

$$PIV = -\hat{V}\sin(\omega t) = -\hat{V}\sin(3\pi/2) = \hat{V}$$

b) Peak SCR current, $\hat{I}$:
In the circuit of **Figure 6.11** the peak current through each SCR will be the same as the peak of the load current, I_L, because each SCR is in series with the load during its conduction interval. Therefore;

$$\hat{I} = I_L$$

c) SCR RMS current, $\hat{V}$**:**
In the circuit of **Figure 6.11** the rms current of each SCR will be the same as the rms equivalent of *half* the load current waveform, because each diode conducts the load current for only half of each cycle. Therefore;

$$I_{rms} = \frac{I_L}{\sqrt{2}}$$

d) Available turn off time, t_q .
In the circuit of **Figure 6.11** the SCR will be reverse biased only during the part of the negative half cycle of $\hat{V}\sin(\omega t)$ when the opposite SCR is turned on, i.e. during;

$$\pi + \alpha \le \omega t_q \le 2\pi$$

And therefore:

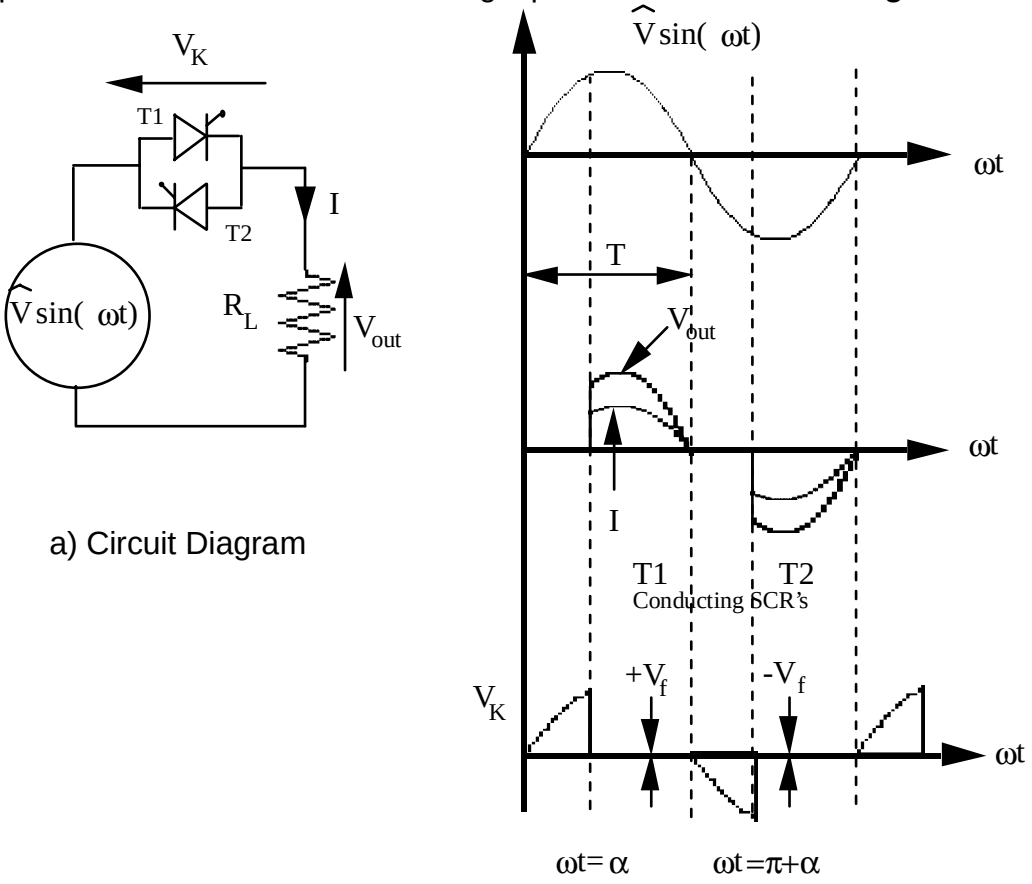
$$t_q = (\pi - \alpha)/\omega$$

Note that the available turn off time for this circuit decreases with increasing α and will go to zero as α approaches π.

6.3 AC PHASE CONTROL CIRCUITS

6.3.1 Single Phase AC Controller

The simplest form of AC controller is a single phase circuit shown in **Figure 6.12.**



a) Circuit Diagram

b) Voltage and Current Waveforms

Figure 6.12 Single Phase AC Controller

This circuit operates exactly like two back to back phase controlled rectifier circuits. Two such back to back SCR's are commonly fabricated into a single device called a TRIAC. However for the purposes of circuit analysis it is more convenient to consider the device as two independent SCR's. SCR T1 is turned on during the positive half cycle of $\hat{V}\sin(\omega t)$ and SCR T2 is turned on during the negative half cycle of $\hat{V}\sin(\omega t)$. Each SCR is turned on at a phase angle of α and thus the effective RMS value of the AC output can be controlled by controlling α. This circuit is commonly used as a light dimmer.

The performance parameters for a single phase AC controller can be determined as follows.

a) RMS value of the output voltage;

$$V_{rms} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi} V_{out}^2 \partial(\omega t)} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi}\left[\hat{V}\sin(\omega t)\right]^2 \partial(\omega t)}$$

$$= \frac{\hat{V}}{2}\left[2 - \frac{2\alpha}{\pi} + \frac{\sin(2\alpha)}{\pi}\right]^{1/2}$$

b) DC value of the output voltage;

$$V_{dc} = \frac{1}{2\pi}\int_{0}^{2\pi} V_{out}\partial(\omega t) = \frac{1}{2\pi}\left[\int_{\alpha}^{\pi}\hat{V}\sin(\omega t)\partial(\omega t) + \int_{\pi+\alpha}^{2\pi}\hat{V}\sin(\omega t)\partial(\omega t)\right]$$

$$= 0$$

Other performance parameters for AC output circuits are; RMS value of the fundamental, RMS value of harmonics, and total harmonic distortion. However phase control circuits are very poor in these respects and are generally used only in applications where harmonics are not important such as lighting and heating applications. For circuits where fundamental content, harmonics etc. are important one usually uses inverters as described in chapter 8.

SCR ratings (Stresses) are;

a) Peak Inverse Voltage, PIV.
PIV occurs across each SCR when it is reverse biased and not conducting. In the circuit shown in **Figure 6.12** SCR T1 will be reverse biased during the negative half of the source voltage waveform until SCR T2 is turned on. The peak of the positive waveform occurs at $\omega t = 3\pi/2$, (provided $\alpha > 3\pi/2$), at which time:

$$PIV = -\hat{V}\sin(\omega t) = -\hat{V}\sin(3\pi/2) = \hat{V}$$

Similarly SCR T2 will be reverse biased during the positive half cycle until SCR T1 is turned on. PIV for this SCR will occur at $\omega t = \pi/2$, (provided a > $3\pi/2$), at which time:

$$PIV = \hat{V}\sin(\omega t) = \hat{V}\sin(\pi/2) = \hat{V}$$

b) Peak current, $\hat{I}$.
In the circuit of **Figure 6.12** the peak current through each SCR will be the same as the peak of the load current, I_L, because each SCR is in series with the load during its conduction interval. Therefore;

$$\hat{I} = \frac{\hat{V}}{R_L}$$

c) SCR RMS current, I_{rms}.

In the circuit of **Figure 6.12** the rms current of each SCR will be the same as the rms of *half* the load current waveform, because each SCR conducts the load current for only half of each cycle. Therefore;

$$I_{rms} = \frac{V_{rms}}{\sqrt{2}R_L} = \frac{\hat{V}}{2\sqrt{2}R_L}\left[2 - \frac{2\alpha}{\pi} + \frac{\sin(2\alpha)}{\pi}\right]^{1/2}$$

Note that for a TRIAC (consisting of both SCR's in a single device the) the TRIAC will conduct during both half cycles and thus will carry all the load current:

$$\text{TRIAC} \quad I_{rms} = \frac{V_{rms}}{R_L} = \frac{\hat{V}}{2R_L}\left[2 - \frac{2\alpha}{\pi} + \frac{\sin(2\alpha)}{\pi}\right]^{1/2}$$

d) Available turn off time, t_q .

In the circuit of **Figure 6.12** the SCR will be reverse biased during the entire negative half cycle of $\hat{V}\sin(\omega t)$, therefore;

$$t_q = \pi/\omega$$

However, the turn off time is composed of two parts. During first part, when neither SCR is conducting;

$$0 \le \omega t \le \alpha$$

The reverse voltage across each SCR will be $\hat{V}\sin(\omega t)$.
During the second part, when SCR T1 is conducting:

$$\alpha \le \omega t \le \pi$$

The reverse voltage across T2 will be equal to V_f, the forward voltage drop across T1.

Example Problem 6.2

A resistive load of 5 Ω requires a voltage control from 0 to 150 Vrms. The available AC supply is 480 V, 60 Hz.

a) Design a TRIAC circuit to provide the required voltage control and determine the following ratings for the TRIAC:

minimum α, maximum α, PIV, $\hat{I}$, I_{rms}

b) Repeat part a) using a transformer as well as a TRIAC.

Solution to Problem 6.2a)

The equivalent circuit for Problem 6.2a) is shown in **Figure 6.13.**

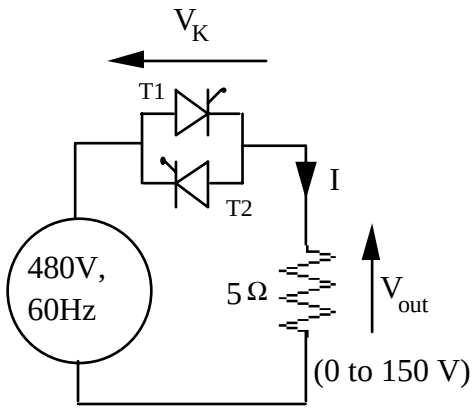


Figure 6.13 Equivalent Circuit for Problem 6.2a

For phase control the output voltage will be:

$$I_{rms} = \frac{\hat{V}}{2R_L}\left[2 - \frac{2\alpha}{\pi} + \frac{\sin(2\alpha)}{\pi}\right]^{1/2}$$

Where;

$$\hat{V} = 480\sqrt{2} = 679$$

For minimum output,

$$V_{rms} = 0$$

And thus;

$$\alpha = \pi$$

For maximum output

$$V_{rms} = 150 = \frac{\hat{V}}{2}\left[2 - \frac{2\alpha}{\pi} + \frac{\sin(2\alpha)}{\pi}\right]^{1/2}$$

$$= \frac{480\sqrt{2}}{2}\left[2 - \frac{2\alpha}{\pi} + \frac{\sin(2\alpha)}{\pi}\right]^{1/2}$$

Rearrange to obtain:

$$\left[2 - \frac{2\alpha}{\pi} + \frac{\sin(2\alpha)}{\pi}\right]^{1/2} = \frac{2\times 150}{480\sqrt{2}} = 0.442$$

Solve for:

$\alpha = 2.34 \quad = 134°$

Therefore;

minimum $\alpha = 2.34 \quad = 134°$

maximum $\alpha = \pi = 180°$

PIV = $\hat{V} = 480\sqrt{2} = 679$

$\hat{I} = \frac{\hat{V}}{R_L} = \frac{480\sqrt{2}}{5} = 136$ Amps, for $0 = \alpha = 90°$

However, at $\alpha = 134°$;

$$\hat{I} = \frac{\hat{V}\sin(\alpha t)}{R_L} = \frac{480\sqrt{2}\sin(134°)}{5} = 97.6 \text{ A}$$

Also;

$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{150}{5} = 30 \quad \text{Amp at } \alpha = 134°,$$

$$= \frac{480}{5} = 96 \quad \text{Amp at } \alpha = 0°$$

Within the normal operating range for this circuit α will not go below its minimum of 134° and $\hat{I}$ will not go above 97.6 A and I_{rms} will not go above 30 A.
However, it is possible that under some transient or unforeseen circumstances, α might go to 0°, in which case the worst case values for $\hat{I}$ and I_{rms} would be 136A and 96 A, respectively.

Solution to Problem 6.2b)

The equivalent circuit for problem 6.2b is shown in **Figure 6.14**.

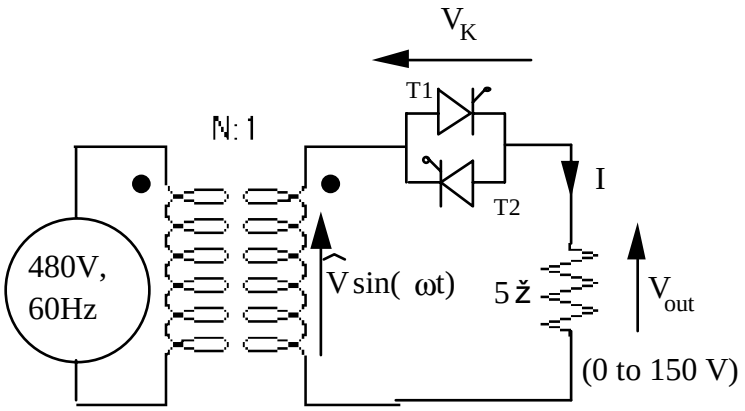


Figure 6.14 Equivalent Circuit for Problem 6.2b

The transformer turns ratio N is chosen such that at minimum α, the output voltage can still reach maximum value;

$$V_{rms} = 150 = \frac{\hat{V}}{2}\left[2 - \frac{2\alpha}{\pi} + \frac{\sin(2\alpha)}{\pi}\right]^{1/2}$$

Substitute for $\alpha = 0$ and solve for;

$$\hat{V} = 150\sqrt{2}$$

Also, from the transformer action;

$$\hat{V} = \frac{480\sqrt{2}}{N}$$

Solve for;

$$N = \frac{480}{150} = 3.2$$

Therefore;

minimum α is 0°, at which V_{rms} = 150 V

maximum α is π , at which V_{rms} = 0 V

PIV = $\hat{V} = 150\sqrt{2}$ = 212 V

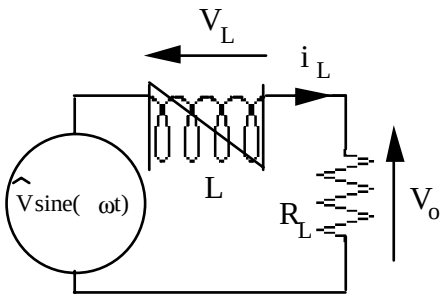
(Note that without the transformer PIV = 679 V)

$$\hat{I} = \frac{\hat{V}}{R_L} = \frac{150\sqrt{2}}{5} = 42.4 \text{ Amps, actual worst case at } \alpha = 0°$$

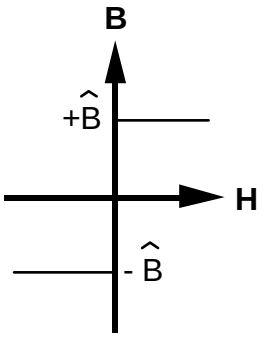
$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{150}{5} = 30 \text{ Amp, actual worst case at } \alpha = 0°$$

6.3.2 Magnetic Amplifier Circuit

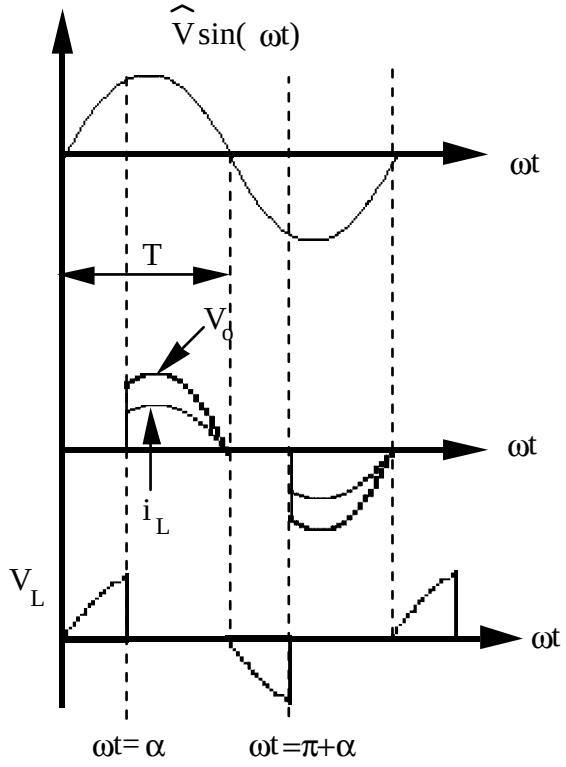
A magnetic amplifier is actually a magnetic switch and is similar in function to an SCR. For historical reasons it has been called a magnetic amplifier. A simplified circuit utilizing a magnetic amplifier is shown in **Figure 6.15**.



a) Circuit Diagram



b) B H curve for the inductor



c) Voltage and Current Waveforms

Figure 15 Magnetic Amplifier Circuit and Waveforms

The inductor L has a non-linear, idealized magnetic characteristic as shown in **Figure 6.15b**. In effect the inductance of L is infinite until it saturates and then becomes zero after it saturates, i.e.:

$L = 8 \quad \text{if } |B| < \hat{B}$

$L = 0 \quad \text{if } |B| = \hat{B}$

Assume that the source voltage is $\hat{V}\sin(\omega t)$ and at t=0, the magnetic flux density, B, in the inductor is:

$B = -\hat{B}$

Therefore, during the positive half cycle of $\hat{V}\sin(\omega t)$;

$L = \infty$ until $B = + \hat{B}$

Therefore the inductor acts like an open circuit and the full source voltage appears across the inductor;

$$v_L(t) = v(t) = \hat{V}\sin(\omega t)$$
$$= N\frac{\partial \Phi}{\partial t} = NA\frac{\partial B}{\partial t}$$

and, assuming an ideal saturation curve as shown in **Figure 6.15b**;

$$i_L(t) = H/N = 0$$

and:

$$v_O(t) = i_L(t)\ R = 0$$

Also the inductor flux will be given by the expression;

$$B(t) = \frac{1}{NA}\int_0^t \hat{V}\sin(\omega t)\partial t$$
$$= \frac{\hat{V}\left[1 - \cos(\omega t)\right]}{\omega NA} - \hat{B}$$

Until the core saturates at $\omega t = \alpha$, which will occur when $B(t) = + \hat{B}$.
Solve for α;

$$\alpha = \cos^{-1}\left(1 - \frac{2\hat{B}\omega NA}{\hat{V}}\right)$$

At this time the core saturates and B(t) can no longer increase, i.e.:

$$\frac{\partial B}{\partial t} = 0$$

Therefore;

$$v_L(t) = NA\frac{\partial B}{\partial t} = 0$$

and;

$$v_O(t) = v(t) - v_L(t) = v(t) = \hat{V}\sin(\omega t)$$

The end result is that during each half cycle the output voltage is zero until the inductor saturates. Once the inductor saturates the output voltage is equal to the input voltage as shown in **Figure 6.15c**. This acts very much like the phase controlled SCR circuit described in section 6.3.1 but instead of a firing angle we have a saturation point. With

an SCR circuit the firing angle can be controlled independently, however in the circuit of **Figure 6.15a** the saturation point is determined by the equation;

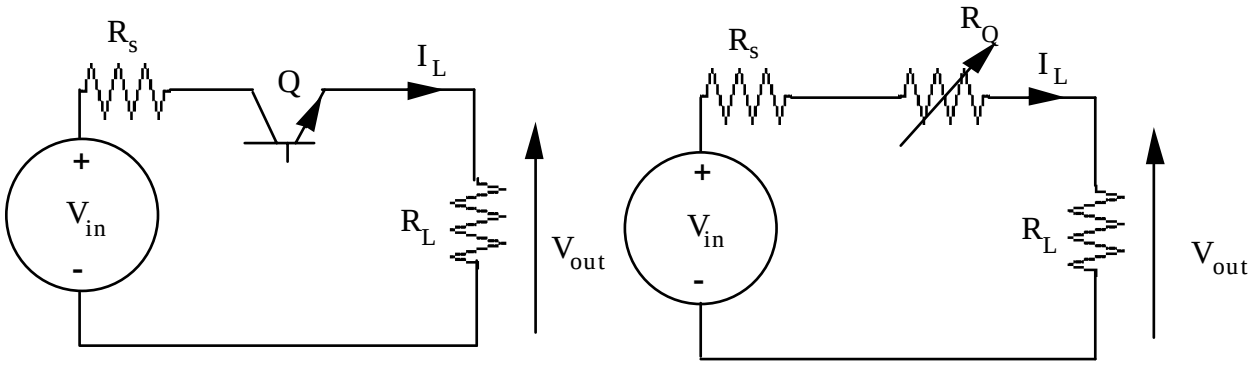
$$\alpha = \cos^{-1}\left(1 - \frac{2\hat{B}\omega NA}{\hat{V}}\right) = \cos^{-1}\left(1 - K\frac{\omega}{\hat{V}}\right)$$

Where K is a constant determined by the inductor characteristics, usually expressed in volt-seconds. With these conditions the output voltage v_O is fixed for a given input voltage waveform $\hat{V}\sin(\omega t)$. One cannot control $v_O(t)$, except by controlling the magnetic flux level in the inductor. Circuits that control this magnetic flux level are called "reset" circuits.

6.4 LINEAR POWER CIRCUITS

6.4.1 Series Regulator

The most common type of linear power circuit is the series regulator. The function of a series regulator is to provide a regulated output voltage in spite of variations in load and/or input voltage. The basic circuit is shown in **Figure 6.16.**



a) Basic series regulator circuit b) Simplified equivalent circuit

Figure 6.16 Series Regulator Circuit

The series element Q may be either a bipolar transistor or a FET or (most often) a complete integrated circuit including feedback loops, error amplifiers, etc. In effect the series element Q functions as a variable series resistor as shown in the equivalent power circuit in **Figure 6.16b**. The effective series resistance of the transistor Q is varied electronically so as to maintain a constant output voltage against changes in input voltage and/or load resistance. The expression for output voltage is:

$$V_{out} = \frac{R_L}{R_Q + R_L + R_S} V_{in}$$

Therefore V_{out} can be controlled by varying R_Q against changes in R_L and/or R_S and/or V_{in} . Note that the above equation is valid for R_S = 0, thus a series regulator will work even if there is no source resistance.

The major design constraints on a series regulator are:

a) Minimum Dropout Voltage, ΔV_{min}

All series regulators require a minimum ΔV to operate, this is called the dropout voltage, ΔV_{min} . Therefore it is necessary to determine the minimum

V that series regulator will be subjected to.
Where;

$$\Delta V_{min} = V_{in} - I_L R_S - V_{out} = V_{in} - \frac{V_{out}}{R_L} R_S - V_{out}$$

For proper circuit operation it is neccessary to determine the *worst case* value of ΔV_{min} from the above expression so that the series regulator will continue to operate for all possible values of V_{in} , R_L , and R_S .

Therefore, for the worst case:

$$\Delta V_{min} = V_{in}\Big|_{min} - I_L \Big|_{max} \times R_S \Big|_{max} - V_{out} = V_{in} \Big|_{min} - \frac{V_{out}}{R_L\Big|_{min}} R_S \Big|_{max} - V_{out}$$

b) Maximum standoff voltage ΔV_{max} :
All series regulators will break down if the

V exceeds a maximum threshold that is referred to as the maximum standoff,

ΔV_{max} . Therefore it is neccessary to determine the maximum

ΔV that the series regulator will be subjected to;
Where;

$$\Delta V_{max} = V_{in} - I_L R_S - V_{out} = V_{in} - \frac{V_{out}}{R_L} R_S - V_{out}$$

For continued circuit operation it is neccessary to determine the *worst case* value of ΔV_{max} from the above expression so that the series regulator will not be damaged for all possible values of V_{in} , R_L , and R_S .

Therefore, for the worst case:

$$\Delta V_{max} = V_{in} \Big|_{max} - I_L \Big|_{min} \times R_S \Big|_{min} - V_{out} = V_{in} \Big|_{max} - \frac{V_{out}}{R_L\Big|_{max}} R_S - V_{out}$$

c) Maximum current rating, $\hat{I}$

The current through the series regulator will always be equal to the the output current I_L because the two elements are in series.
Therefore:

$$\hat{I} = I_L \Big|_{max}$$

d) The power rating, W

All series regulators have a maximum power dissipating capability, W, beyond which the device will be permanently damaged, where:

$$W = \hat{I} \times \Delta V_{max}$$

In some cases the maximum power dissipating capability, W, may be less than given by the above expression especially at high temperatures.

Note that the efficiency of a series regulator is usually poor resulting in high internal heat dissipation which in turn may result in high component temperatures even if the local ambient temperature is room ambient. In such cases the series regulator is often mounted on a heatsink so as to minimize the temperature rise of the component above the local ambient.

The efficiency of a series regulator circuit can be determined;

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} I_{out}}{V_{in} I_{in}}$$

Substitute;

$$I_{out} = I_{in}$$

To obtain:

$$\eta = \frac{V_{out}}{V_{in}}$$

Also the expression for worst case efficiency is:

$$\eta = \frac{V_{out}\Big|_{min}}{V_{in}\Big|_{max}}$$

Example Problem 6-3

You have a power supply that provides 24V±10% at 1 Amp. It has an equivalent internal series resistance of 2.5 ± 0.5 Ω. However, you require 18V with a load variation from 0.1 to 1.0 A.

Determine;

a) the minimum ΔV (drop-out voltage) available for a series regulator
b) the maximum ΔV (stand-off voltage)
c) the efficiency of the series regulator at 24V input and 18V output
d) the worst case power dissipated in the series regulator.

Solution;

a) $\Delta V_{min} = V_{in}\Big|_{min} - I_L\Big|_{max} \times R_S\Big|_{max} - V_{out}$

$= 24 \times .9 - 1 \times 3.0 - 18$

$= 0.6$ V

b) $\Delta V_{max} = V_{in}\Big|_{max} - I_L\Big|_{min} \times R_S\Big|_{min} - V_{out}$

$= 24 \times .1.1 - 0.1 \times 2.0 - 18$

$= 8.2$ V

c) $\eta = \dfrac{V_{out}}{V_{in}} = \dfrac{18}{24} = 0.75$

d) $P_Q = I_L \Delta V = I_L\left[V_{in} - I_L R_S - V_{out}\right] = I_L V_{in} - I_L^2 R_S - I_L V_{out}$

and;

$\dfrac{\partial P_Q}{\partial I_L} = V_{in} - 2I_L R_S - V_{out} = 0$ for maximum P_Q

Solve for:

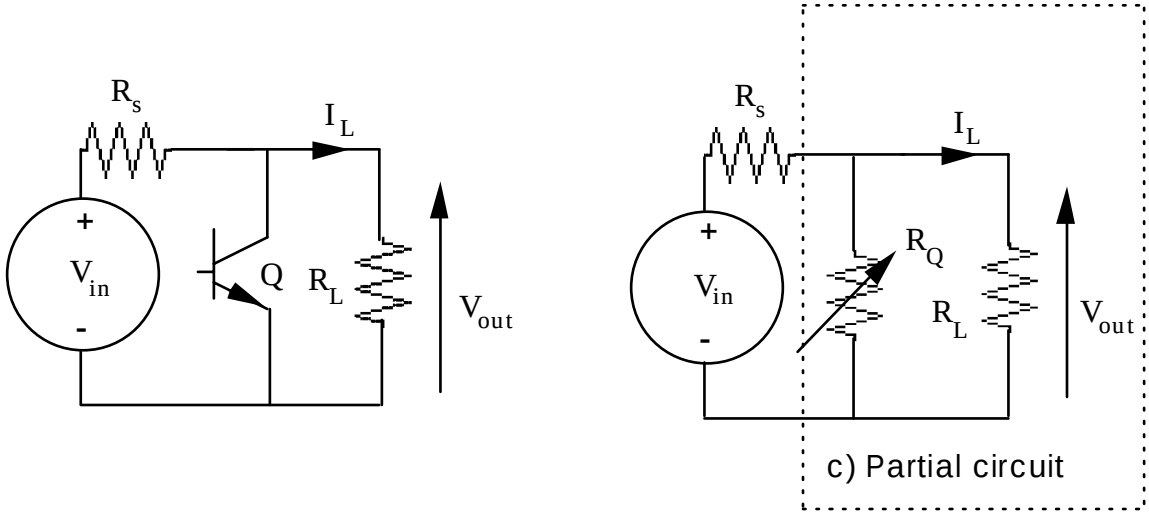
$$I_L = \frac{V_{in}\Big|_{max} - V_{out}}{2R_S\Big|_{min}} = \frac{24\times1.1-18}{2\times(2.5-0.5)} = 2.1 \text{ A}$$

However $0.1 < I_L < 1.0$

$\therefore\ P_{Qmax} = 1.0\left[24\times1.1-1.\times2.0-18\right] = 6.4$W

6.4.2 Shunt Regulator

The shunt regulator is similar to the series regulator described in the preceding section. The major difference is that a shunt regulator will only operate if the source voltage has a significant source resistance. A shunt regulator is efficient only for relatively small variations in loading. The basic circuit is shown in **Figure 6.17.**



a) Basic shunt regulator circuit b) Simplified equivalent circuit

Figure 6.17 Shunt Regulator Circuit

The shunt element Q may be either a bipolar transistor or a FET or (most often) a complete integrated circuit including feedback loops, error amplifiers, etc. In effect the shunt element Q functions as a variable shunt resistor as shown in the equivalent power circuit in **Figure 6.17b**. The effective shunt resistance of the transistor Q is varied electronically so as to maintain a constant output voltage against changes in input voltage and/or load resistance. The expression for output voltage is:

$$V_{out} = \frac{R_Q \| R_L}{R_Q \| R_L + R_S} V_{in} = \frac{R_Q R_L}{R_Q R_L + R_Q R_S + R_S R_L} V_{in}$$

Therefore V_{out} can be controlled by varying R_Q against changes in R_L and/or R_S and/or V_{in} provided that $R_S > 0$, thus a shunt regulator will *not work if there is no source resistance.*

The major design constraints on a shunt regulator are:

a) Minimum Shunt Current, I_{Qmin}

All shunt regulators require a minimum I_{Qmin} to operate. Therefore it is necessary to determine the minimum current, I_{Qmin} , that the shunt regulator will be subjected to.

Where;

$$I_{Qmin} = \frac{V_{in} - V_{out}}{R_S} - I_L = \frac{V_{in} - V_{out}}{R_S} - \frac{V_{out}}{R_L}$$

For proper circuit operation it is neccessary to determine the *worst case* value of I_{Qmin} from the above expression so that the shunt regulator will continue to operate for all possible values of V_{in} , R_L , and R_S .

Therefore, for the worst case:

$$I_{Qmin} = \frac{V_{in}\Big|_{min} - V_{out}}{R_S\Big|_{max}} - I_L\Big|_{max} = \frac{V_{in}\Big|_{min} - V_{out}}{R_S\Big|_{max}} - \frac{V_{out}}{R_L\Big|_{min}}$$

b)Maximum current rating, $\hat{I}_Q$

The current through the shunt regulator must not exceed the maximum allowable for the device. The expression for $\hat{I}_Q$ can be determined from the above equation for I_{Qmin} but substituting for the worst case conditions that result in maximum shunt current;

$$\hat{I}_Q = \frac{V_{in}\Big|_{max} - V_{out}}{R_S\Big|_{min}} - I_L\Big|_{min} = \frac{V_{in}\Big|_{max} - V_{out}}{R_S\Big|_{min}} - \frac{V_{out}}{R_L\Big|_{max}}$$

d) The power rating, W

All shunt regulators have a maximum power dissipating capability, W, beyond which the device will be permanently damaged, where:

$$W = V_{out} \times \hat{I}_Q$$

In some cases the maximum power handling capability, W, may be less than given by the above expression especially at high temperatures.

Note that the efficiency of a shunt regulator is usually even lower than for a series regulator resulting in high internal heat dissipation which in turn may result in high component temperatures even if the local ambient temperature is room ambient. In such cases the shunt regulator is often mounted on a heatsink so as to minimize the temperature rise of the component above the local ambient.

The efficiency of a shunt regulator circuit can be determined;

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} I_{out}}{V_{in} I_{in}}$$

The above expression gives the efficiency of the overall circuit, output power vs total input power from the source voltage V_{in} .

In some applications a more relevant efficiency is that of the partial circuit shown in **Figure 6.17c**. In this case the efficiency can be determined as;

$$\eta' = \frac{P_{out}}{P'_{in}} = \frac{V_{out} I_{out}}{V'_{in} I_{in}}$$

Substitute;

$$V'_{in} = V_{out}$$

To obtain:

$$\eta' = \frac{I_{out}}{I_{in}} = \frac{I_L}{I_{in}}$$

Example Problem 6-4

You have a power supply that provides 24V±10% at 1 Amp. It has an equivalent internal series resistance of 2.5 ± 0.5 Ω. However, you require 18V with a load variation from 0.1 to 1.0 A.

Determine;

a) The minimum current rating for a shunt regulator
b) The maximum current rating for a shunt regulator
c) The worst case power dissipation in the shunt regulator
d) The overall efficiency of the shunt regulator circuit under the conditions in part c)

Solution to Example 6-4

a) $$I_{Qmin} = \frac{V_{in}\Big|_{min} - V_{out}}{R_S\Big|_{max}} - I_L\Big|_{max}$$

$= (24 \times 0.9 - 18)/3.0 - 1.0$
$= 0.2$ A

b) $$\hat{I}_Q = \frac{V_{in}\Big|_{max} - V_{out}}{R_S\Big|_{min}} - I_L\Big|_{min}$$

$= (24 \times 1.1 - 18)/2.0 - 0.1$
$= 4.1$ A

c) $W = V_{out} \times \hat{I}_Q$
$= 18 \times 4.1$
$= 73.8$ W

d) $$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} I_{out}}{V_{in} I_{in}}$$

Where:

$V_{out} = 18$ V
$V_{in} = V_{in}\Big|_{max} = 24 \text{ X } 1.1 = 26.4$ V

$$I_{out} = I_L\Big|_{min} = 0.1\ A$$

$$I_{in} = \frac{V_{in}\Big|_{max} - V_{out}}{R_S\Big|_{min}} = (24 \times 1.1 - 18)/2.0 = 4.2\ A$$

Therefore;

$$\eta = \frac{18 \times 0.1}{26.4 \times 4.2} = 0.016$$

6.4.3 Zener Diode Regulator

The Zener diode regulator, (usually referred to as simply a Zener regulator), is similar to the shunt regulator described in the preceding section. The major difference is that a Zener diode functions as voltage source rather than a variable resistor. The basic circuit diagram for Zener regulator is shown in **Figure 6.18.**

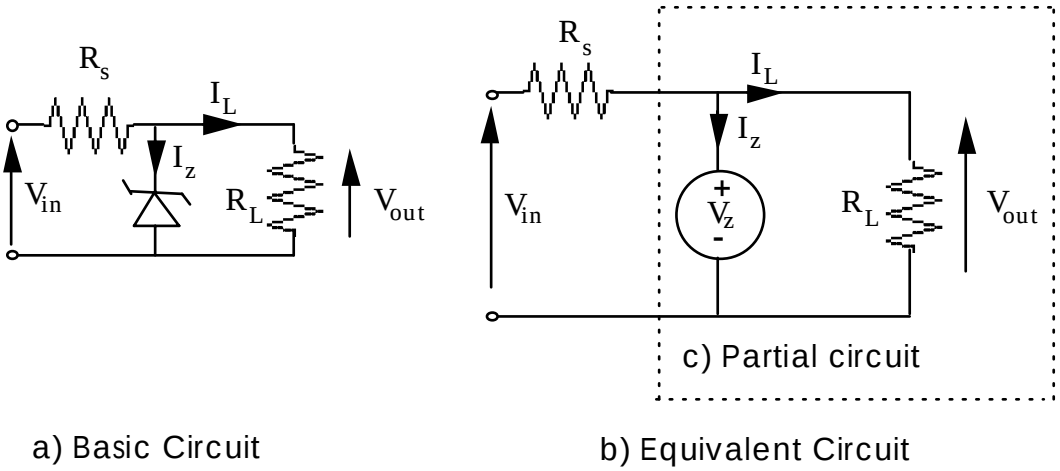


Figure 6.18 Zener Diode Regulator

Just as a shunt regulator, the Zener regulator will only operate if the source voltage has a significant source resistance. The equivalent power circuit for a Zener diode regulator is shown in **Figure 6.18b**. The output voltage is equal to the Zener voltage, V_Z . However V_Z will vary by a significant percentage depending on the current through the device and the percentage tolerance of the particular device. In general V_Z will be at the maximum of its tolerance when the current is at its maximum and V_Z will be at its minimum when the current is at its minimum. It can be seen from **Figure 6.18b**, that V_Z and thus also V_{out} can be different from V_{in} only if $R_S > 0$, thus a Zener regulator will *not work if there is no source resistance.*

The major design constraints on a Zener diode regulator are:

a) Minimum Zener Current, I_Z

All Zener diodes require a minimum I_Z to maintain the Zener voltage. Therefore it is necessary to determine the minimum current, I_Z , that the Zener diode will be subjected to.

Where;

$$I_Z = \frac{V_{in} - V_{out}}{R_S} - I_L = \frac{V_{in} - V_{out}}{R_S} - \frac{V_{out}}{R_L}$$

For proper circuit operation it is neccessary to determine the *worst case* value of I_Z from the above expression so that the Zener diode regulator will continue to operate for all possible values of V_{in} , R_L , V_{out} and R_S .

Therefore, for the worst case:

$$I_Z = \frac{V_{in}\Big|_{min} - V_Z\Big|_{min}}{R_S\Big|_{max}} - I_L\Big|_{max} = \frac{V_{in}\Big|_{min} - V_Z\Big|_{min}}{R_S\Big|_{max}} - \frac{V_Z\Big|_{min}}{R_L\Big|_{min}}$$

Note that the minimim value of V_Z is substituted in the above equation because when I_Z is at its minimum V_Z will also be at its minimum.

b)Maximum current rating, $\hat{I}$

The current through the Zener diode must not exceed the maximum allowable for the device. The expression for $\hat{I}$ can be determined from the above equation for I_Z but substituting for the worst case conditions that result in *maximum* shunt current;

$$\hat{I} = \frac{V_{in}\Big|_{max} - V_Z\Big|_{max}}{R_S\Big|_{min}} - I_L\Big|_{min} = \frac{V_{in}\Big|_{max} - V_Z\Big|_{max}}{R_S\Big|_{min}} - \frac{V_Z\Big|_{max}}{R_L\Big|_{max}}$$

Note that the maximum value of V_Z is substituted in the above equation because when the Zener current is at its maximum V_Z will also be at its maximum.

d) The power rating, W

All Zener diodes have a maximum power dissipating capability, W, beyond which the device will be permanently damaged, where:

$$W = V_Z \times \hat{I}$$

In some cases the maximum power handling capability, W, may be less than given by the above expression especially at high temperatures.

Note that the efficiency of a Zener diode regulator is usually even lower than for a shunt regulator resulting in high internal heat dissipation which in turn may result in high component temperatures even if the local ambient temperature is room ambient. In such cases the Zener diode is often mounted on a heatsink so as to minimize the temperature rise of the component above the local ambient.

The efficiency of a Zener diode regulator circuit can be determined;

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} I_{out}}{V_{in} I_{in}} = \frac{V_Z I_L}{V_{in} I_{in}}$$

The above expression gives the efficiency of the overall circuit, output power vs total input power from the source voltage V_{in} .

In some applications a more relevant efficiency is that of the partial circuit shown in **Figure 6.18c**. In this case the efficiency can be determined as;

$$\eta' = \frac{P_{out}}{P'_{in}} = \frac{V_{out} I_{out}}{V'_{in} I_{in}}$$

Substitute;

$$V'_{in} = V_{out}$$

To obtain:

$$\eta' = \frac{I_{out}}{I_{in}} = \frac{I_L}{I_{in}}$$

Example Problem 6-5

You have a power supply that provides 24V±10% at 1 Amp. It has an equivalent internal series resistance of 2.5 ± 0.5 Ω. However, you require 18V with a load variation from 0.1 to 1.0 A. You can only afford a 10% Zener which you plan to use to build a Zener regulator.

Determine;

a) The minimum current rating for the Zener
b) The maximum current rating for a Zener
c) The worst case power dissipation in the Zener
d) The overall efficiency of the Zener diode regulator circuit under the conditions in part c)

Solution to Example 6-5

a) $$I_Z = \frac{V_{in}\Big|_{min} - V_Z\Big|_{min}}{R_S\Big|_{max}} - I_L\Big|_{max}$$

$= (24 \times 0.9 - 18 \times 0.9)/3.0 - 1.0$
$= 0.8A$

b) $$\hat{I}_Q = \frac{V_{in}\Big|_{max} - V_Z\Big|_{max}}{R_S\Big|_{min}} - I_L\Big|_{min}$$

$= (24 \times 1.1 - 18 \times 1.1)/2.0 - 0.1$
$= 3.25\ A$

c) $W = V_Z \times \hat{I}_Q$
$= (18 \times 1.1) \times 3.25$
$= 64.35\ W$

d) $$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} I_{out}}{V_{in} I_{in}}$$

Where:

$$V_{out} = V_Z\Big|_{max} = 18 \times 1.1 = 19.8\ V$$

$$V_{in} = V_{in}\Big|_{max} = 24 \text{ X } 1.1 = 26.4 \text{ V}$$

$$I_{out} = I_L\Big|_{min} = 0.1 \text{ A}$$

$$I_{in} = \frac{V_{in}\Big|_{max} - V_{out}}{R_S\Big|_{min}} = (24 \times 1.1 - 19.8)/2.0 = 3.3 \text{ A}$$

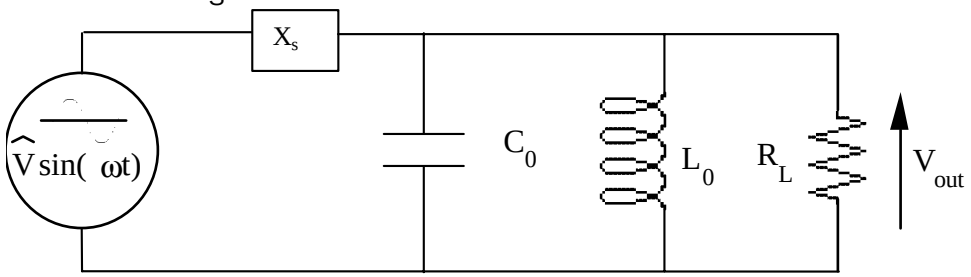
Therefore;

$$\eta = \frac{19.8 \times 0.1}{26.4 \times 3.3} = 0.023$$

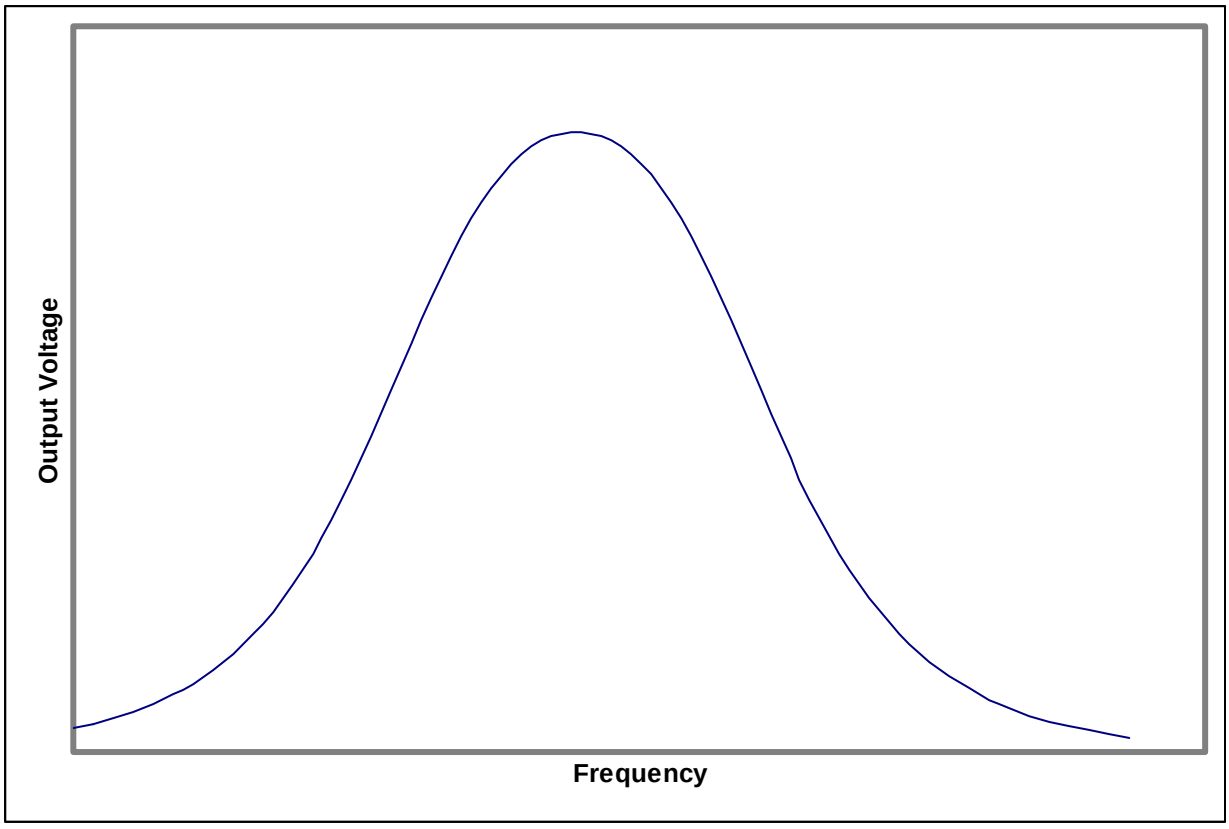
6.4.4 Resonant Circuits

Resonant circuits are used in some advanced power supplies to provide a means of controlling the output voltage by varying the internal switching frequency. There are many different types of resonant circuits used in such power supplies but most fall into one of two basic types: Parallel Resonant and Series Resonant.

The simplified basic schematic for a Parallel Resonant circuit is shown in **Figure 6.19**. The series impedance, X_S , can be either an inductor or a capacitor.



a) Parallel Resonant Circuit



b) Typical Output Voltage vs Frequency Curve

Figure 6.19 Parallel Resonant Circuit

The voltage source V_S is usually a square wave but as a first approximation can be represented as:

$$V_S = \hat{V} \sin(\omega t)$$

Where ω is variable.
The resonant elements are L_0 and C_0 which together with R_L form a tank circuit which has a characteristic resonant frequency ω_r , where;

$$\omega_r = \sqrt{\omega_0^2 - \alpha^2}$$

and

$$\omega_0^2 = \frac{1}{L_0 C_0}$$

and

$$\alpha = \frac{1}{2R_L C_0}$$

For best results the circuit elements are designed such that the tank circuit is *underdamped*, i.e.

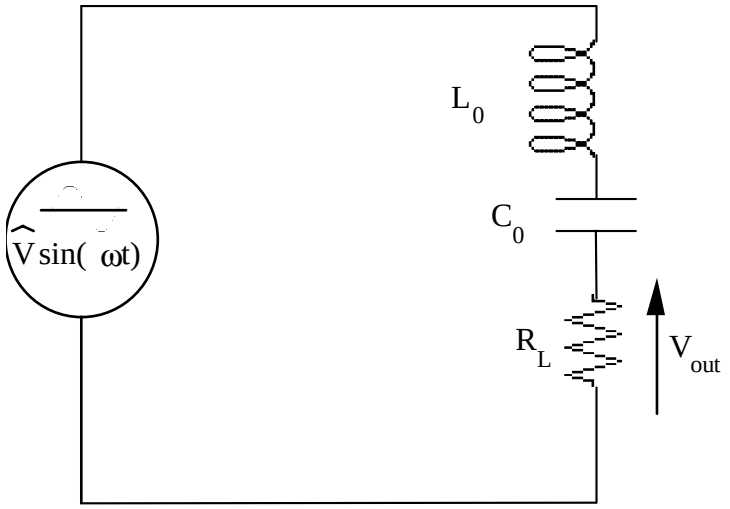
$$\omega_0 > \alpha$$

The output voltage can then be controlled by varying the switching frequency ω as shown in **Figure 6.19b**. It can be seen that there are two regions in the frequency domain in which the output voltage V_{out} can be controlled;

a) Under resonant region
In this region V_{out} increases with increasing frequency. This region is generally easier to operate in by starting at very low frequency and ramping up.

b) Over resonant region
In this region V_{out} decreases with increasing frequency.

The simplified basic schematic for a Series Resonant circuit is shown in **Figure 6.20**.



a) Series Resonant Circuit

Figure 6.20 Series Resonant Circuit

The operation of this circuit is similar to the Parallel Resonant circuit. The major difference is in the nature of the resonant frequency parameter α. For a Series Resonant circuit;

$$\alpha = \frac{R_L}{2L_0}$$

Other than that, the equations and operating regions, etc. are basically similar.

Advantages of resonant circuits

Resonant circuits are used because, if properly designed, the current through the switching semiconductors, (transistors, diodes, SCR's) naturally goes to zero. This reduces switching losses in the semiconductors and results in higher efficiency. Also reduced switching losses enables the circuit to operate at higher switching frequencies. This generally results in physically smaller energy storage components such as inductors, transformers and capacitors.

Disadvantages of resonant circuits

Parallel resonant circuits inherently have high circulating currents through the resonant elements;

$$I_L \approx I_C \approx QI_{out}$$

Similarly, in a Series resonant circuit the voltages across the resonant elements are high;

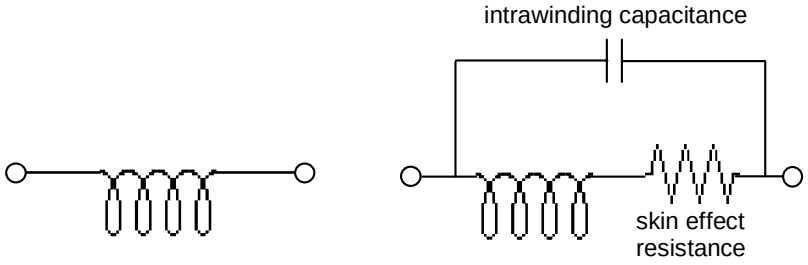
$$V_L \approx V_C \approx QV_{out}$$

Where Q is the quality factor for the resonant circuit and is typically between 5 and 10. Thus the current or voltage ratings of the resonant inductors and capacitors are several

times higher than the output voltage or current. This combined with the higher operating frequency means that the inductors and capacitors have to be special high performance and low loss types which are usually more expensive.

6.4.5 High Frequency Inductor Model

The basic high frequency model of an inductor is shown in **Figure 6.21**. The high frequency model includes the addition of a capacitor and resistor. The capacitor represents the intrawinding capacitance; the capacitance between adjacent turns of wire from the same winding. This is usually a few picofarads which can be significant for the very high frequency components of a switching waveform. The resistance represents the effective increased resistance of the wire at high frequencies. At high frequencies the current through a wire does not penetrate the entire cross sectional area of the wire but instead is confined to a relatively thin 'skin depth'. This skin depth is inversely related to frequency and thus the wire resistance increases for higher frequencies. This is called the "skin effect".



a) Basic Inductor b) High Frequency Equivalent Circuit

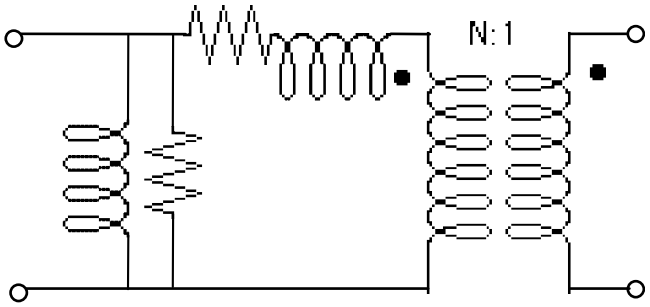
Figure 6.21 High Frequency Equivalent Circuit for an Inductor

6.4.6 High Frequency Transformer Model

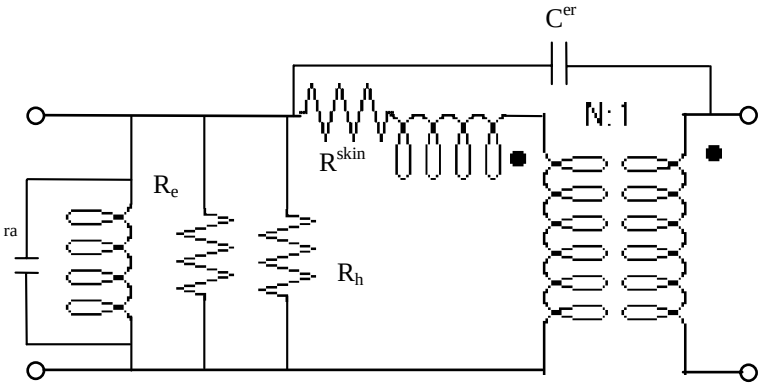
The basic high frequency model of a transformer is shown in **Figure 6.22**. The high frequency model includes the addition of several capacitors and resistors. The capacitor, C^{ra}, represents *intrawinding* capacitances. The capacitance between adjacent turns of wire from the same winding. The capacitor, C^{er}, represents *interwinding* capacitances. The capacitance between adjacent turns of wire from different windings. It is significant to note that the same construction techniques that are used to reduce interwinding capacitance, (increasing separation of primary and secondary windings), will also tend to increase leakage inductance.

The resistor, R^{skin}, represents the effective increased resistance of the wire due to the skin effect. The resistors, R_h and R_e, represents the core losses due to hysteresis and eddy currents respectively, both of which increase with increasing frequency, f, but in different degrees:

$$R_h \approx \frac{K_h}{f} \quad \text{and} \quad R_e \approx \frac{K_e}{f^2}$$



a) Basic Transformer

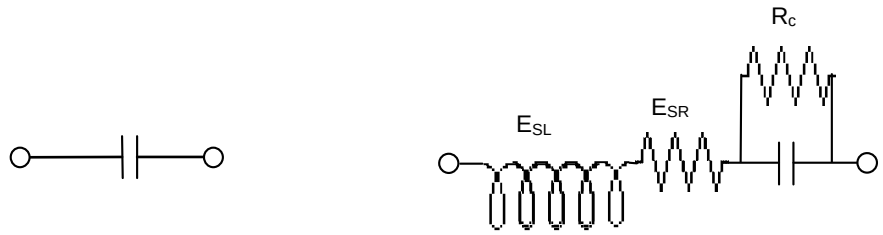


b) High Frequency Equivalent Circuit

Figure 6.22 High Frequency Equivalent Circuit for a Transformer

6.4.7 High Frequency Capacitor Model

The basic high frequency model of a capacitor is shown in **Figure 6.23**. The high frequency model includes the addition of resistive and inductive elements. The E_{SR} is the equivalent series resistance which represents the increased resistance of the internal foil due to the skin effect. The E_{SL} is the equivalent series inductance of the internal foil. This is usually only a few picoHenries but can be significant for the high frequency components of a switching waveform. The R_C represents the internal dissipation in the dielectric which can be significant at high frequencies.



a) Basic Capacitor b) High Frequency Equivalent Circuit

Figure 6.23 High Frequency Equivalent Circuit for a Capacitor

6.5 PROBLEMS

6.5.1 Series Regulators

1. Design a 5V, 10A power supply using a series regulator with a minimum drop-out voltage of 3V. The minimum input voltage is V_S and the maximum input voltage is $2V_S$. Draw the equivalent circuit and determine;
a)Minimum value for V_S. (8V)
b)The series regulator ratings in Watts and ΔV_{max}. (110W)
c)The power supply efficiency at minimum and maximum input. (62.5%,31.25%)

2. Design a SERIES REGULATOR to operate from a 12V (nominal) car battery. The requirements are;

Input Voltage: 10.5 Vdc to 14.8 Vdc
Output Current: 3A max.
Output Voltage: 5 Vdc

Draw the basic circuit diagram and determine;
a) The minimum and maximum ΔV across the series regulator. (5.5V, 9.8V)
b) The maximum power dissipated in the series requlator. (29.4W)
c) The regulator efficiency at worst case. (33.8%)
d) The value of series resistance required to reduce the maximum power dissipation in the series regulator by half. (1.63Ω)
e) The overall efficiency, at worst case, in part d). (33.8%)

3. Design a series regulator to produce a regulated 5 V output with load variations of 10 mA to 100 mA. The available source is a "9 V" battery that varies from 9 V down to 5.4 V and has an internal resistance of 2 Ω.
Determine ΔV_{min}, ΔV_{max}, P_{Qmax} for the series regulator and P_{Bmax}, the maximum power dissipated within the battery. (0.2V, 4.98V, 0.38W, 0.02W)

4. Design series regulator to produce an output of 15V, 2.5A. The input voltage varies from V_S to $2V_S$. Draw the basic circuit diagram and determine the following:
a) The minimum value for V_S if the series regulator dropout
voltage is 3 Volts minimum. (18V)
b) The maximum value for V_S if the series regulator power limit
75 Watts maximum. (22.5V)
c) The regulator efficiency, for the worst case value of V_S,
under maximum input voltage conditions, assuming maximum load. (33%)

5. Design a SERIES REGULATOR to operate from a 24V (nominal) car battery. The requirements are;

Input Voltage: 19 Vdc to 32 Vdc
Output Current: 0.5A to 1.5A
Output Voltage: 5 Vdc

Draw the basic circuit diagram and determine;

a) The minimum and maximum ΔV across the series regulator. (12V, 27V)

b) The maximum power dissipated in the series requlator. (40.5W)

c) The regulator efficiency at worst case. (15.6%)

d) The maximum value of additional series resistance, (in ohms and watts), that could be added and still keep the ΔV to 3V minimum across the series regulator. (7.33Ω, 16.5W)

6. Design a 5V, 10A power supply using a series regulator with a minimum drop-out voltage of ΔV_{min} . The minimum input voltage is V_S and the maximum input voltage is $2V_S$. Determine the following:

a)The minimum value for V_S as a function of ΔV_{min} . $(5 + \Delta V_{min})$

b)The maximum value for V_S as a function of ΔV_{max} . $(2.5 + 0.5\Delta V_{max})$

c)ΔV_{max} and worst case power supply efficiency if ΔV_{min} =2V. (9V, 35.7%)

d)ΔV_{min} and worst case power supply efficiency if ΔV_{max} =10V. (2.5V, 33%)

6.5.2 Shunt Regulators

7. Design a shunt regulator to produce 12V from an input of 24Vdc ± 5Vdc. The load is 1.0A ± 10%. The source resistance is 5 ohms. Draw the basic circuit diagram and determine;
a)The shunt regulator rating in amps and watts. (2.5A, 30W)
b)The power supply efficiency at nominal load and maximum input voltage. (29%)

8. Design a SHUNT REGULATOR to produce 24V from an input of 48Vdc ±8Vdc. The load varies from 0 to 0.5 A. The source resistance is 25 ohms. Draw the basic circuit diagram and determine;
a)The shunt regulator rating in max. amps and max. watts. (1.28A, 30.7W)
b)The overall efficiency of output power versus total power drawn from the input voltage source, at maximum load and maximum input. (16.7%)

6.5.3 Zener Regulators

9. Design a zener voltage regulator to produce 12V from an input of 24Vdc ± 5Vdc. The load is 0.1A ± 10%. The minimum zener current is 100mA. Draw the basic circuit diagram and determine;
a)The series resistor rating in ohms and watts. (7Ω, 41.3W)
b)The zener diode rating in amps and watts. (1.53A,18.3W)
c)The regulator efficiency at nominal load and maximum input voltage. (15.24%)

10. Design a Zener regulator to produce a regulated 5 V output with load variations of 10 mA to 100 mA. The available source is a "9 V" battery that varies from 9 V down to 5.4 V and has an internal resistance of 2 Ω.
Determine I_{Zmin} , I_{Zmax} , P_{Zmax} and P_{Bmax} , the maximum power dissipated within the battery. (0.1A, 1.99A, 9.95W, 8W)

11. Design a ZENER VOLTAGE REGULATOR to produce 24V from an input of 48Vdc ±8Vdc. The load varies from 0 to 0.5 A. The source resistance is 25 ohms. Determine the following;
a)The worst case series resistor dissipation in watts. (40.96W)
b)The zener diode rating in amps and watts. (1.28A, 30.7W)
c)The overall efficiency of output power versus total power drawn from the input voltage source, at maximum load and maximum input.

12. Design a zener diode voltage regulator to operate from a 24V (nominal) battery. The requirements are;

Input Voltage: 19 Vdc to 32 Vdc
Output Current: 0 to 25 mA
Output Voltage: 5 Vdc
Series resistance: 150Ω minimum
Zener Current: 3 mA minimum

Determine the following:
a) The maximum value of series resistance. (500Ω)
b) The worst case zener diode rating in amps and watts. (0.180A, 0.9W)
c) The worst case power dissipation in the series resistance. (4.86W)

6.5.4 SCRs and Triacs

13. Design a 200Vac, 50A, power supply for a resistive load using a transformer and two SCR's in a TRIAC configuration. The input voltage is 115V ± 15V, 60 Hz. Assume an ideal transformer and zero forward voltage drop in the SCR's. Draw the basic circuit diagram and determine;
a)The transformer turns ratio and maximum output voltage from the transformer. (0.5, 260V)
b)The minimum and maximum firing angles. (0°, 81.7°)
c)The SCR voltage and current ratings. (377 PIV, 50A rms, 94.3A peak)

14. Design a 150Vdc, 6A power supply using a FULL BRIDGE SCR. The input voltage IS 60Hz AC with a minimum RMS value of V_S and the maximum RMS value of $2V_S$. Determine the following;
a)Minimum value for V_S . (166.7V)
b)The maximum value for V_S if the PIV for each SCR is 500V. (176.8V)
c)The minimum and maximum firing angles for each of the above cases. (0°, 90°: 27.8°, 93.3°)

15. Design a 50Vdc, 10Adc, power supply for a DC motor drive using a centre-tapped transformer and two SCR's in a half-bridge configuration. The input voltage is 115V ± 15V, 60 Hz. Assume an ideal transformer and zero forward voltage drop in the SCR's. Draw the basic circuit diagram and determine;
a)The transformer turns ratio and maximum output voltage. (1.8, 72.2V)
b)The minimum and maximum firing angles. (0°, 57.5°)
c)The SCR voltage rating. (204 PIV)

16. Design a 500Vdc power supply for a resistive load of 12 ohms, using a centre tapped transformer, and two SCR's. The nominal input voltage is 115V ± 15V, 60 Hz. Assume an ideal transformer can be designed with any turns ratio. Determine the following;
a) The transformer turns ratio, and maximum output voltage. (0.18, 722)
b) The minimum and maximum firing angles for the SCR's. (0°, 57.4°)
c) The peak voltage, peak current, and rms current for the SCR's at the MAXIMUM FIRING ANGLE as determined in part b). (2042 PIV, 85A peak, 54.3A rms)

17. Design a 600Vdc, 10KW power supply for a resistive load using a transformer and four SCR's in a full bridge configuration. The input voltage varies from 176 to 265 Vac. Assume an ideal transformer can be designed with any turns ratio. Determine the following:

a) The transformer turns ratio, and maximum output voltage. (0.293, 903V)
b) The minimum and maximum firing angles for the SCR's. (0°, 95°)
c) The PIV, peak current, and rms current for the SCR's at the MAXIMUM FIRING ANGLE as determined in part b). (1278 PIV, 35.4A peak, 16.7A rms)

18. Design a 600Vac, 10KW power supply for a resistive load using a transformer and a TRIAC. The input voltage varies from 176 to 265 Vac. Assume an ideal transformer can be designed with any turns ratio. Determine the following:
a) The turns ratio and maximum output voltage of the transformer. (0.293, 903V)
b) The minimum and maximum firing angles for the triac. (0°, 95°)
c) The PIV, peak current, and rms current for the triac at the MAXIMUM FIRING ANGLE as determined in part b). (1278 PIV, 35.4A peak, 16.7A rms)

6.5.5 SCR Commutation

19. In the commutation circuit shown in Figure 6.5.1. SCR's Q_1 and Q_4 are conducting the load current at $t=0^-$. SCR's Q_2 and Q_3 are turned on at t=0. Assume that the load current, I_O is constant, and the initial capacitor voltage is $+V_C$. Determine the following:

a) The voltage waveform for voltage across the capacitor, $v_C(t)$. (V_C - I_O t/C)

b) The output voltage waveform $v_O(t)$. ($2V_S$ - I_O t/C)

c) The available turn off time, t_q , for Q_1 and Q_4 . (CV_C /I_O)

d) The PIV for Q_1 and Q_4 . (V_C)

e) The reapplied dV/dt for Q_1 and Q_4 . (I_O /C)

Figure 6.5.1 A capacitor bridge commutation circuit.

20. In the circuit shown in Figure 1, SCR T1 is turned on at t=0. Initial conditions are: $V_c(0) = -V_S$ and i(0) = 0. Assume ideal SCR, capacitor and inductor. Determine:

a) The expressions for i(t) and $V_c(t)$. ($2V_S$ sin(ωt)/ωL, $2V_S$ {1-cos(ωt)}-V_S)

b) The time at which the SCR turns off. ($p/\sqrt{LC}$)

c) The end value for $V_c(t)$. ($3V_S$)

Figure 6.5.2

21.You are required to design a power supply to provide a constant current of 100 Adc using a Half Bridge Centre-Tapped SCR Circuit. The input voltage is 120Vac, 1000 Hz. The SCR's require a turn of time of125 µs. Determine the maximum value of negative output voltage possible with these SCR's. (135V)