solantro®
SEMICONDUCTOR CORP.

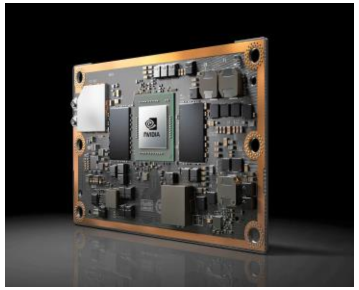
Current Mode Control Using IXC2

November 16, 2018

High Growth Applications

Applications in Data Center, Automotive, Automation, Renewables:

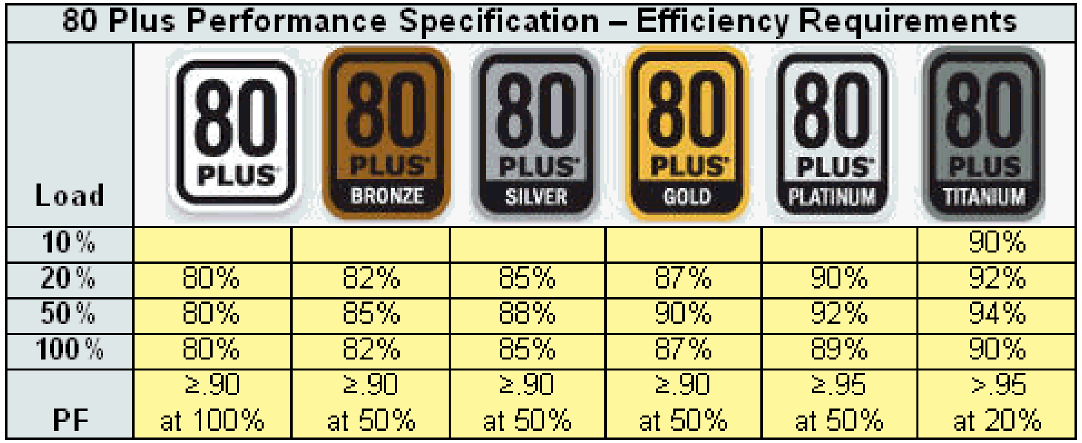
1. AC/DC - Power-Factor-Corrected- Bridgeless & Interleaved
2. DC/DC - LLC, Half-Bridge, Phase-Shifted Full-Bridge, etc.
3. Charging - On-board (EV), Charge Stations, Off-grid
4. Inverters - Bi-Directional, Automotive, UPS and Storage
5. Heavy Industrial - Electrified Equipment, HVAC, Welding




Smart Power supply

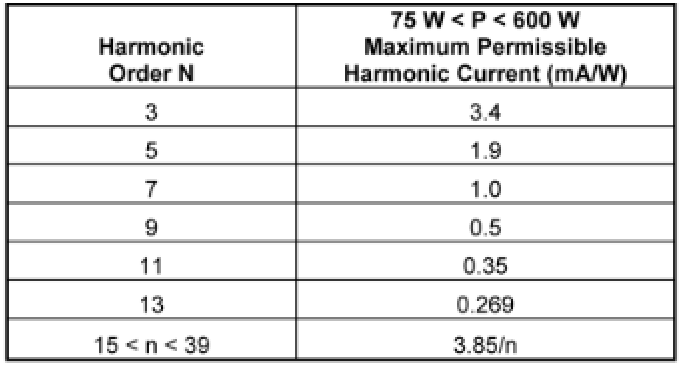
- 80 PLUS® standards
- ENERGY STAR®
- EN61000-3-2



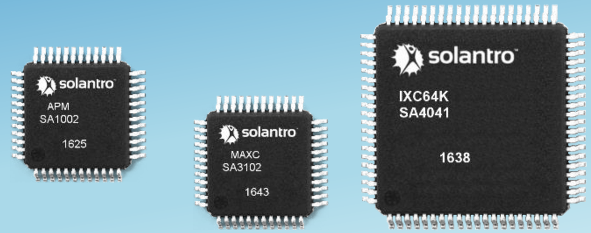
80 Plus Performance Specification – Efficiency Requirements

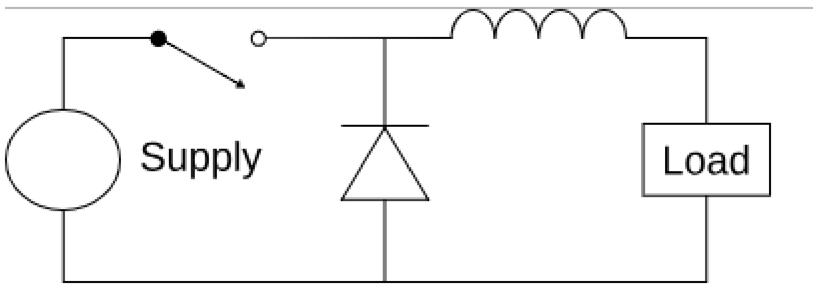
Load	80 PLUS	80 PLUS BRONZE	80 PLUS SILVER	80 PLUS GOLD	80 PLUS PLATINUM	80 PLUS TITANIUM
10 %						90%
20 %	80%	82%	85%	87%	90%	92%
50 %	80%	85%	88%	90%	92%	94%
100 %	80%	82%	85%	87%	89%	90%
PF	≥.90 at 100%	≥.90 at 50%	≥.90 at 50%	≥.90 at 50%	≥.95 at 50%	>.95 at 20%

ENERGY STAR

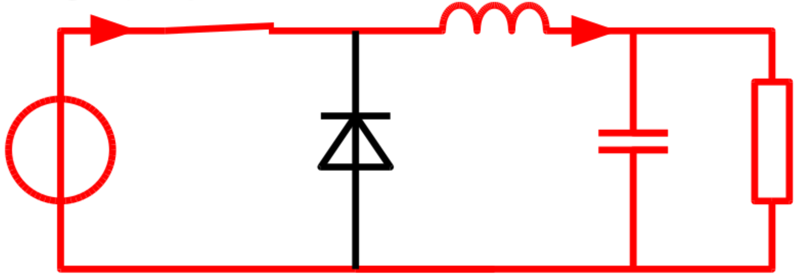


Harmonic Order N	75 W < P < 600 W Maximum Permissible Harmonic Current (mA/W)
3	3.4
5	1.9
7	1.0
9	0.5
11	0.35
13	0.269
15 < n < 39	3.85/n

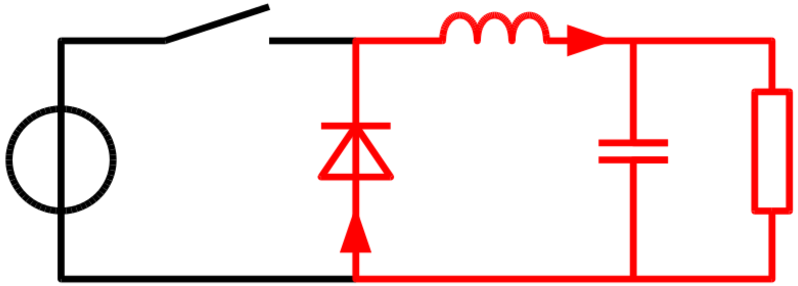


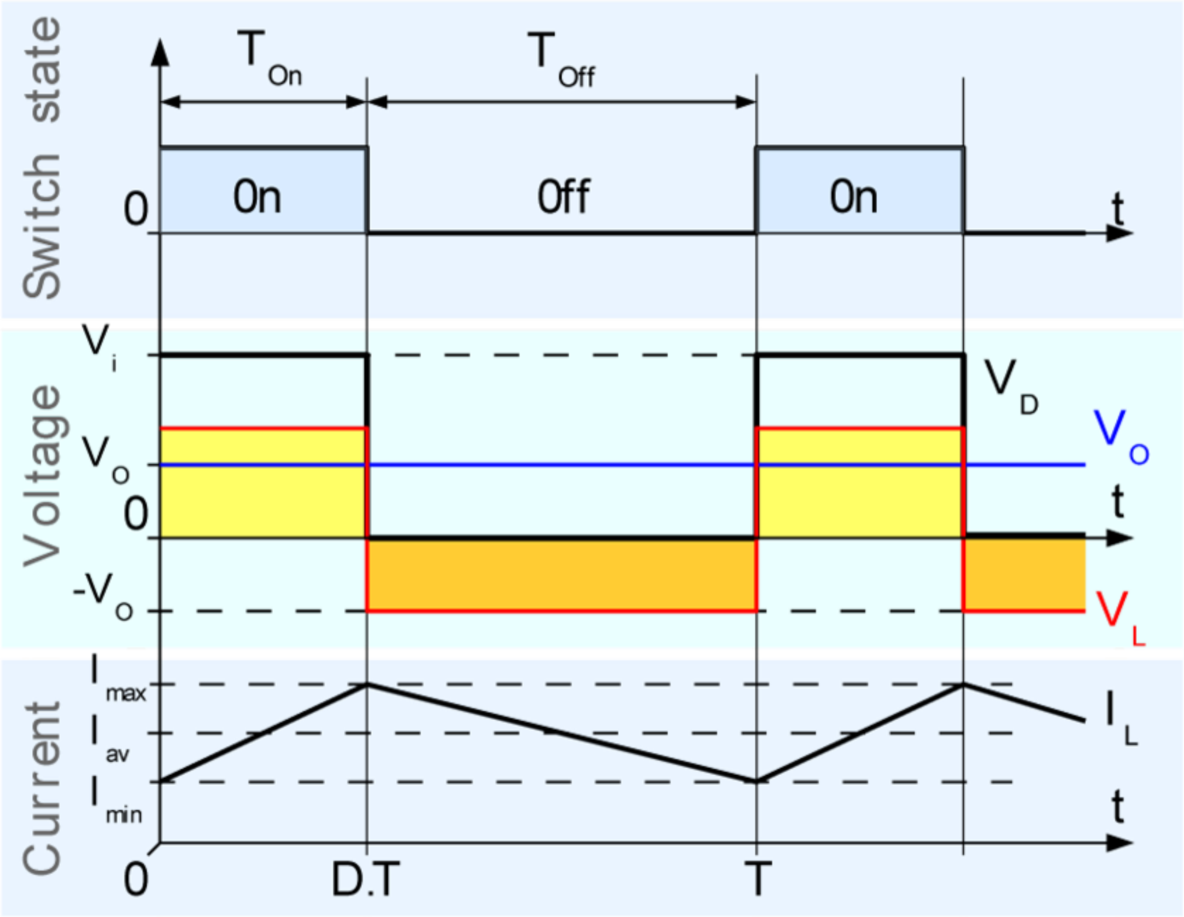


On-State



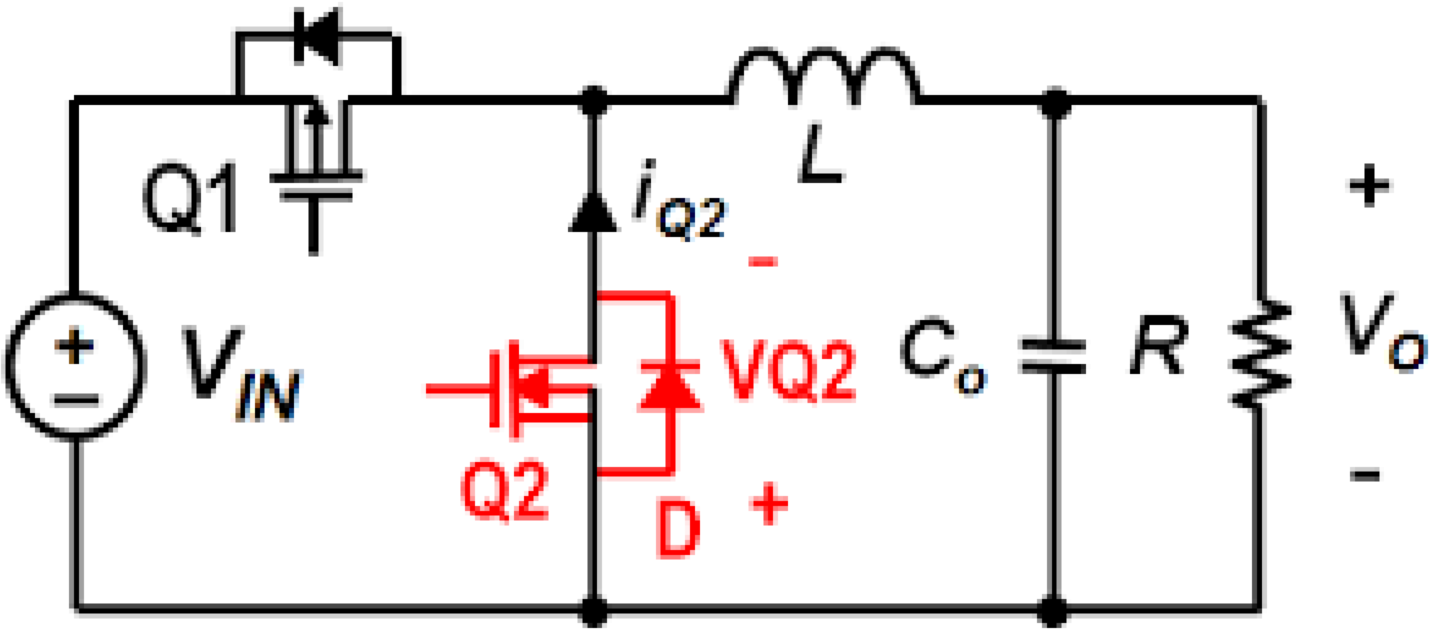
Off-State

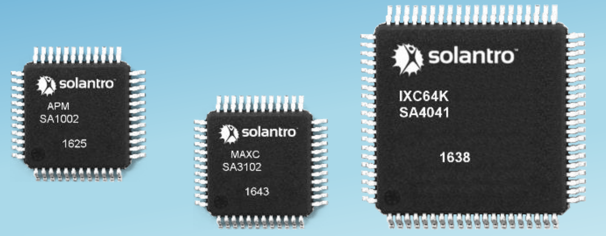


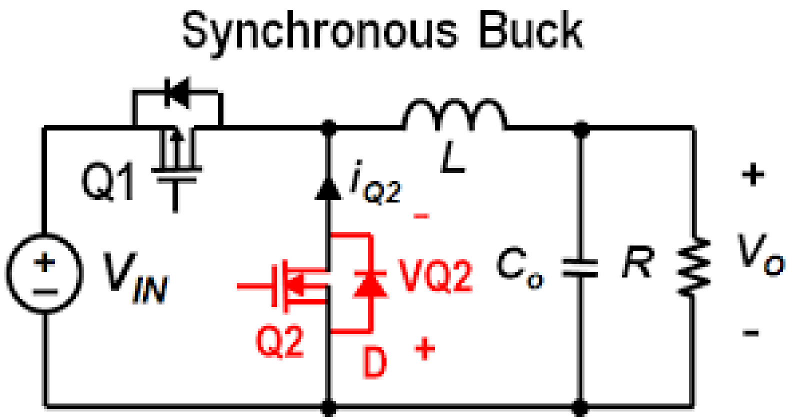


$$D = \frac{V_0}{V_{in}}$$

Synchronous Buck



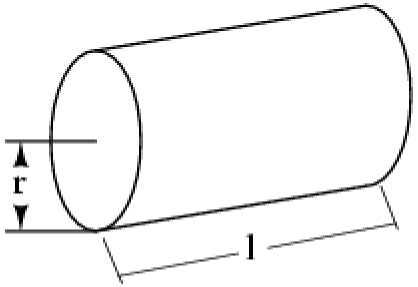




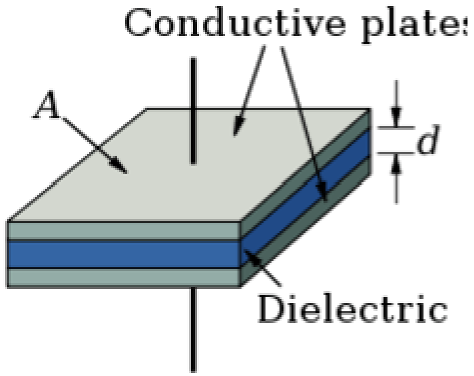
$$L = f(1/f_{SW})$$

$$C = f(1/f_{SW})$$

$$L = \frac{N^2 \mu A}{l}$$



$$C = \frac{\varepsilon_0 A}{d}$$



The need for high-voltage, high power density devices operating at high frequencies and junction temperatures higher than 150 °C is growing, especially for advanced power

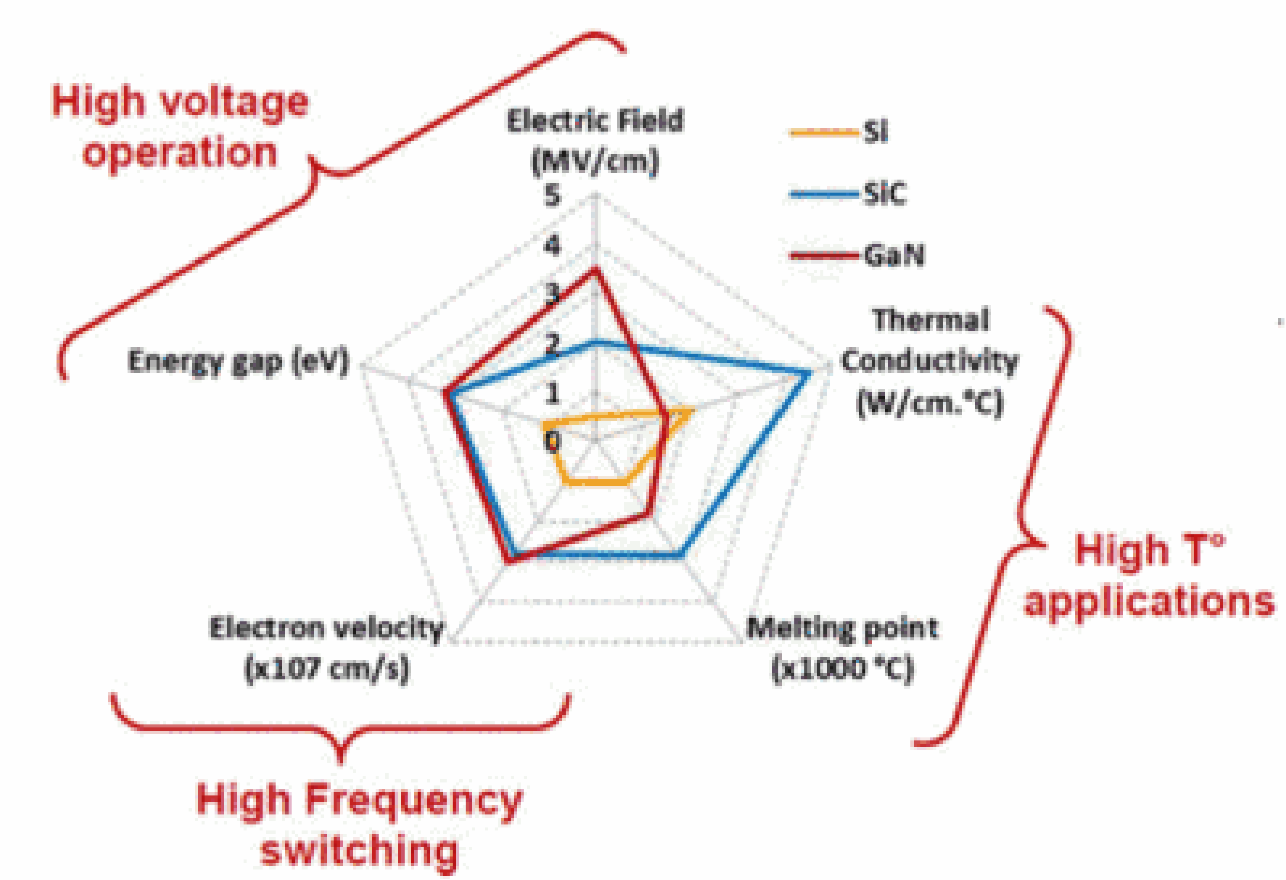
Table 1. Physical properties for various semiconductors.

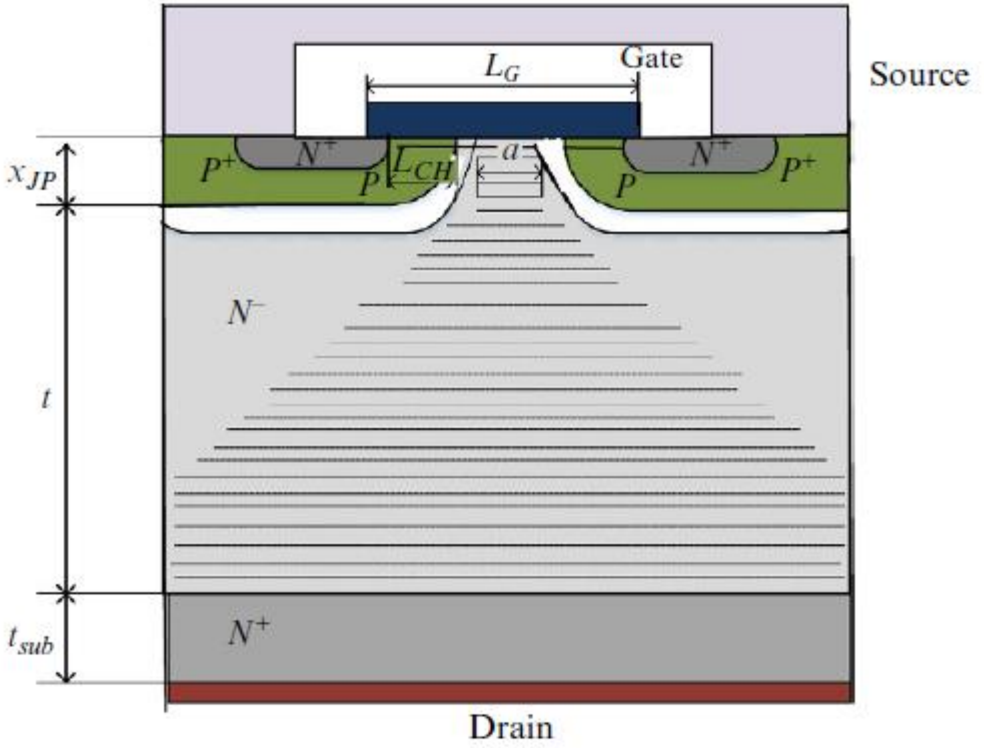
Material	E_G, eV	E_C, MV/cm	n_i, cm^{-3}	ε_r	μ_r, cm^2/V/s	v_{SAT}, 10^7 cm/s	σ_T, W/m/K	CTE, ppm/K
Si	1.1	0.3	10^{10}	11.9	1400	1.02	130	2.6
GaAs	1.424	0.4	2.1×10^6	13.1	8500	2.0	55	5.73
3C-SiC	2.36	1	10		≤ 800	2.0	360	3.8
4H-SiC	3.23	3-5	8.2×10^{-9}	10.1	≤ 900	2.0	370	5.12
6H-SiC	3.0	3-5	2.3×10^{-6}	9.66	≤ 400	2.0	490	4.3-4.7
GaN wurtzite	3.39	3-5	1.9×10^{-10}	9	≤ 1000	2.2	130	3.2-5.6
GaN zinc blende	3.2							
Diamond	5.45	5.6	1.6×10^{-27}	5.5	1900	2.7	600-2,000	0.8

$$R_{SP-ON} = \frac{1.716\times10^{-6}\,\varepsilon_r BV^{2.5} E_G^{-3}}{\mu_n}$$

$$R_{SP-ON} = \frac{3.351\times10^{-3}\,BV^{2} E_G^{-6}}{\varepsilon_r \mu_n}$$

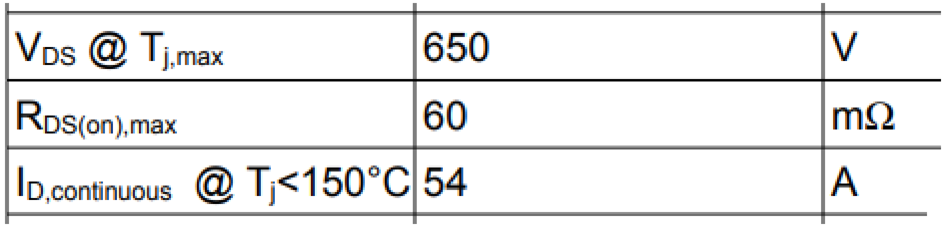
$$R_{SP-ON} = \frac{8.725\times10^{-3}\,BV^{2} E_G^{-7.5}}{\varepsilon_r \mu_n}$$


High voltage operation
Electric Field (MV/cm)
5
4
3
2
1
0
Si
SiC
GaN
Thermal Conductivity (W/cm.°C)
Energy gap (eV)
Electron velocity (x107 cm/s)
Melting point (x1000 °C)
High T° applications
High Frequency switching

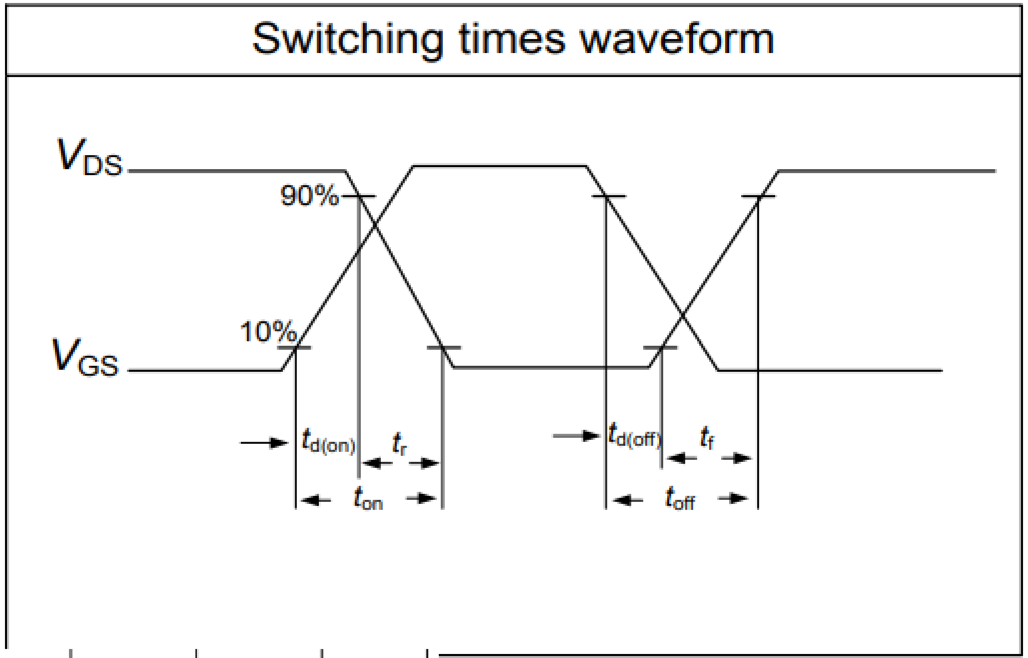

Gate
L_G
Source
x_{JP}
P^+
N^+
P
L_{CH}
a
N^+
P
P^+
N^-
t
t_{sub}
N^+
Drain

CoolMOS™ C7

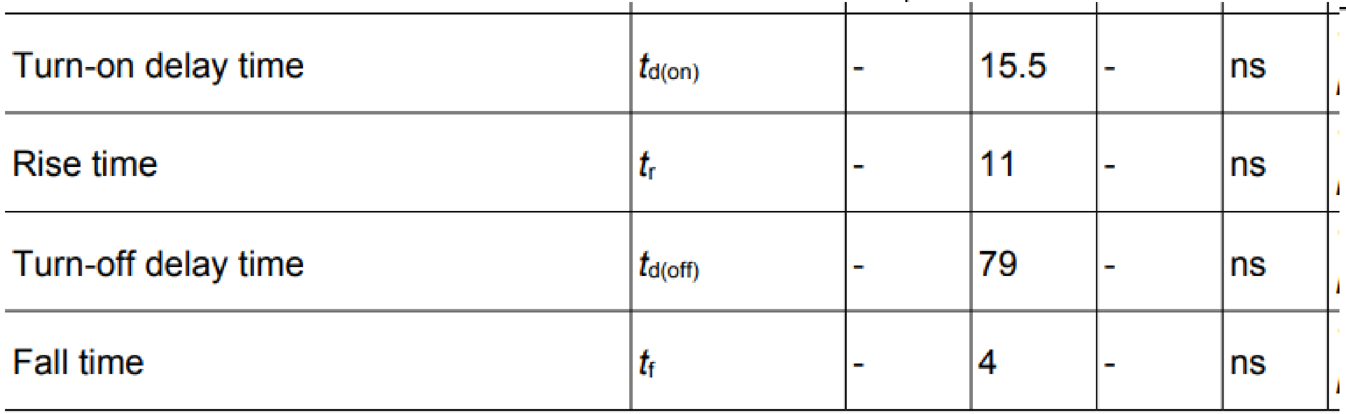
600V CoolMOS™ C7 Power Transistor
IPB60R060C7



V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	60	mΩ
$I_{D,continuous}$ @ T_j<150°C	54	A

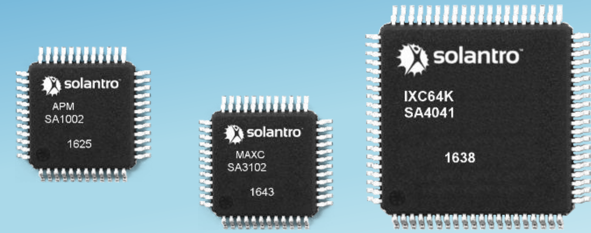


Switching times waveform



Turn-on delay time	$t_{d(on)}$	-	15.5	-	ns
Rise time	t_r	-	11	-	ns
Turn-off delay time	$t_{d(off)}$	-	79	-	ns
Fall time	t_f	-	4	-	ns

https://www.infineon.com/dgdl/Infineon-IPB60R060C7-DS-v02_00-EN.pdf?fileId=5546d46258fc0bc1015917ac25385ea1



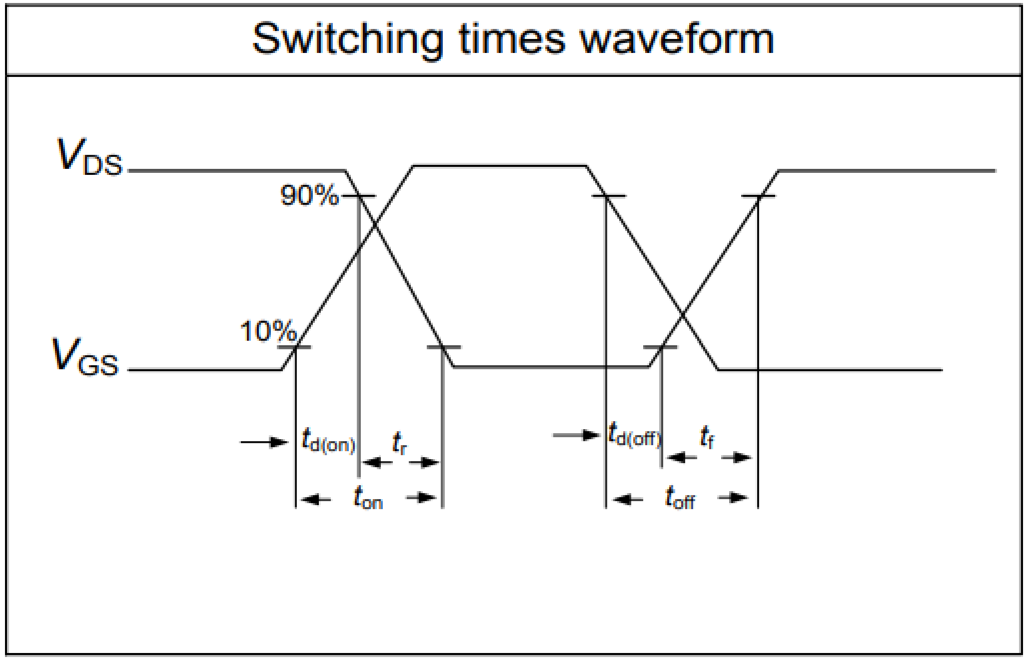
C3M0065090J

Silicon Carbide Power MOSFET

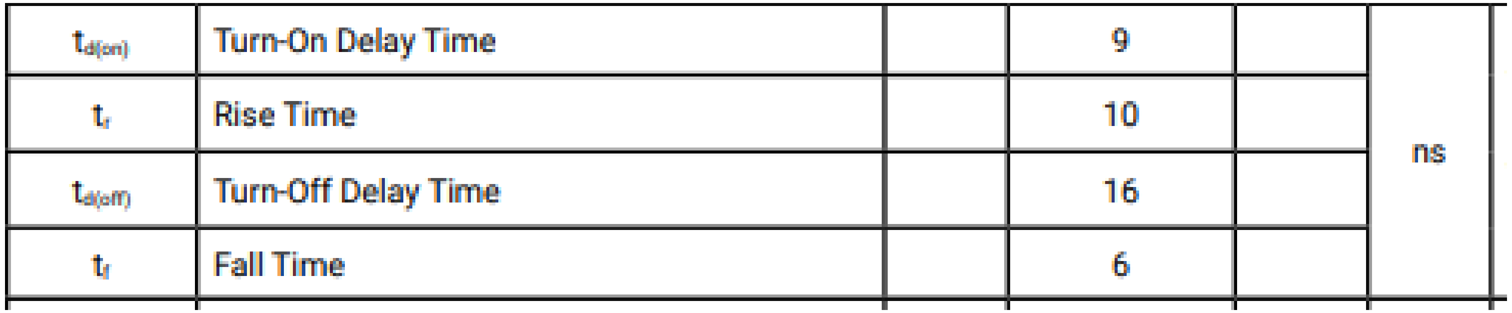
C3M^{TM} MOSFET Technology

N-Channel Enhancement Mode

V_{DS}	900 V
$I_{D\ @\ 25^{\circ}C}$	35 A
$R_{DS(on)}$	65 mΩ

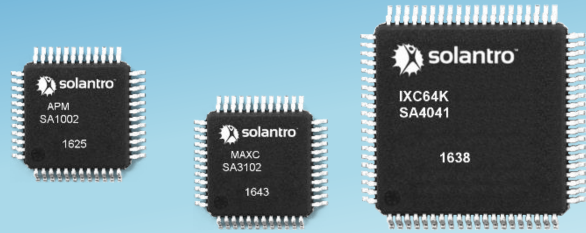


Switching times waveform



$t_{d(on)}$	Turn-On Delay Time		9		ns	
t_r	Rise Time		10			
$t_{d(off)}$	Turn-Off Delay Time		16			
t_f	Fall Time		6			

https://www.wolfspeed.com/downloads/dl/file/id/145/product/1/c3m0065090j.pdf



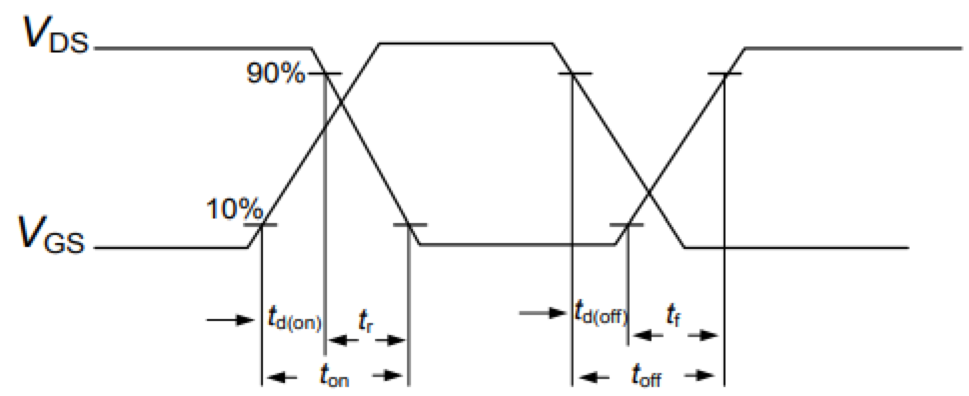
GaN Systems

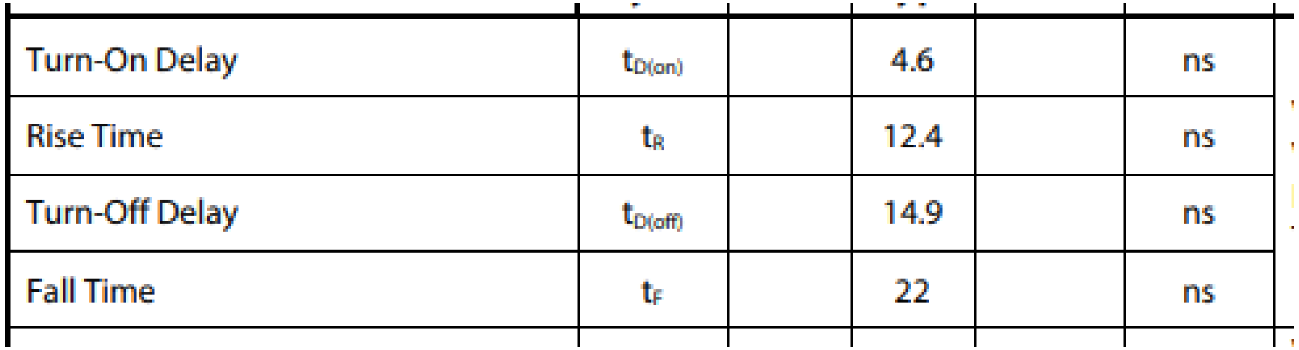
GS66516T

Top-side cooled 650 V E-mode GaN transistor

- 650 V enhancement mode power switch
- Top-side cooled configuration
- $R_{DS(on)} = 25\ m\Omega$
- $I_{DS(max)} = 60\ A$

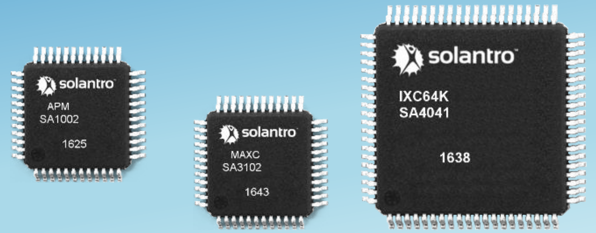
Switching times waveform





Turn-On Delay	$t_{D(on)}$		4.6		ns
Rise Time	t_R		12.4		ns
Turn-Off Delay	$t_{D(off)}$		14.9		ns
Fall Time	t_F		22		ns

https://gansystems.com/wp-content/uploads/2018/04/GS66516T-DS-Rev-180422.pdf



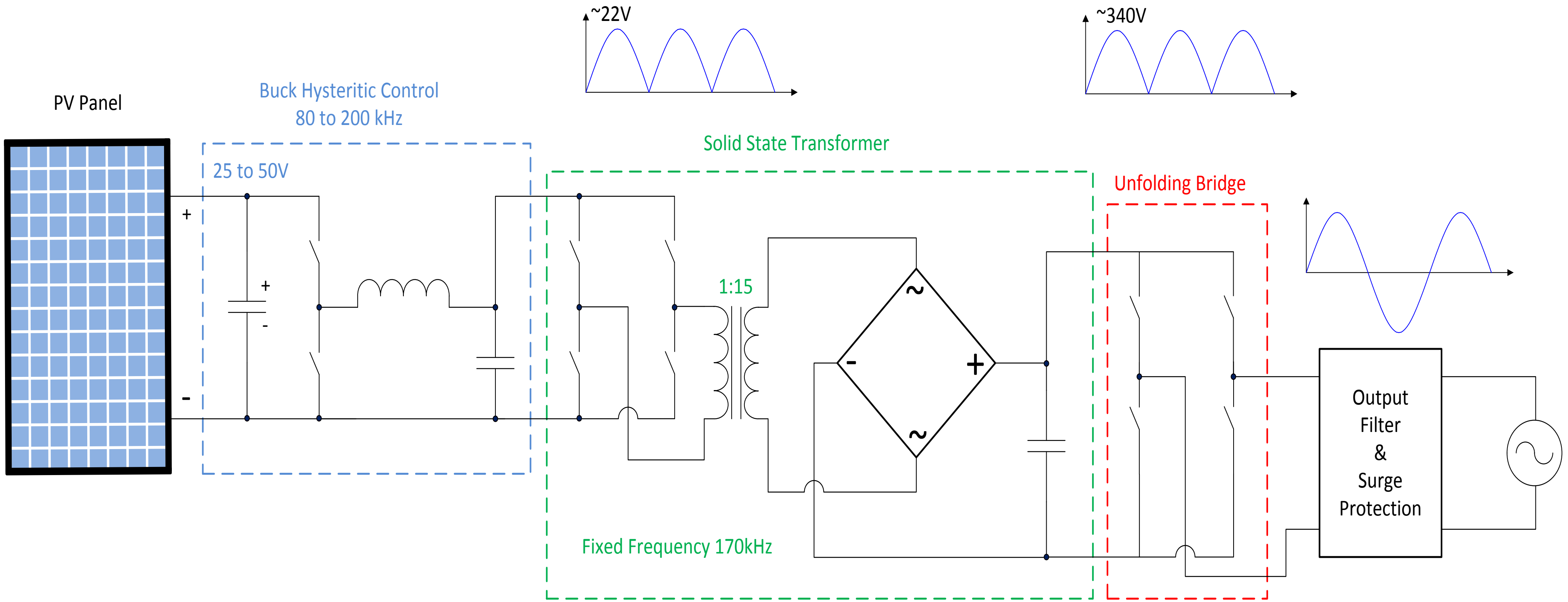
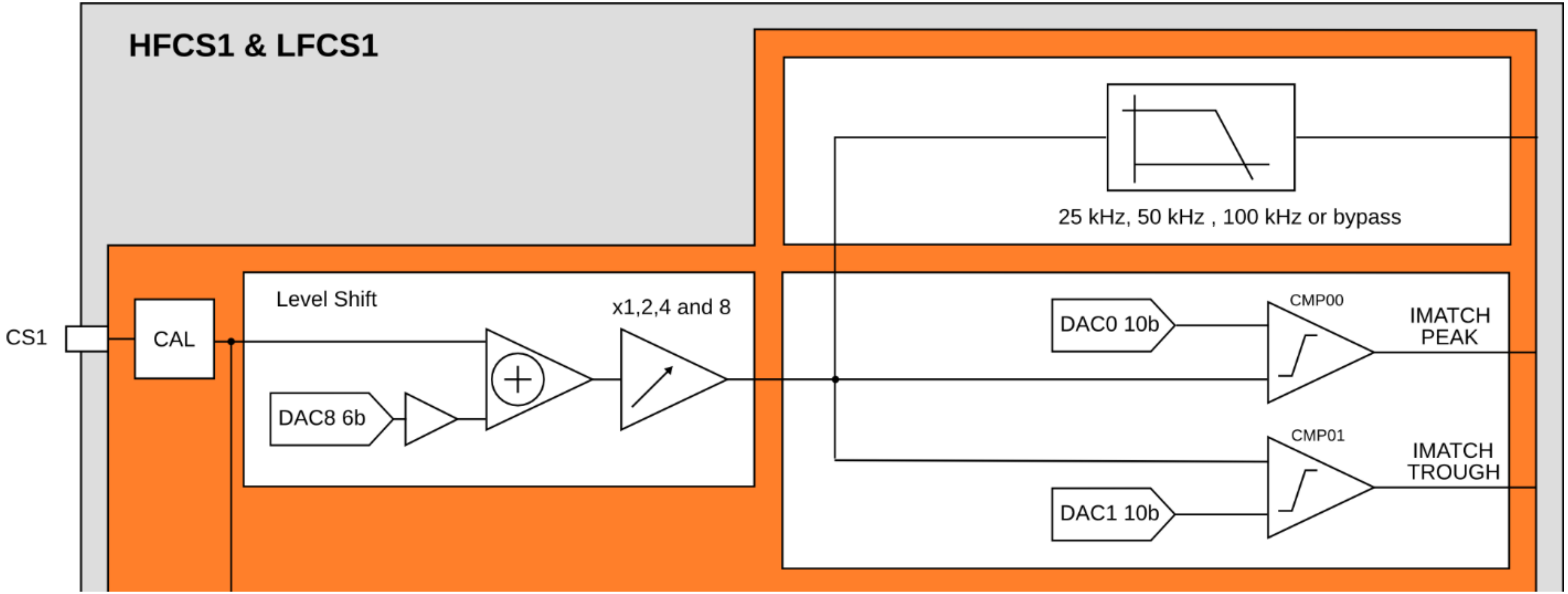
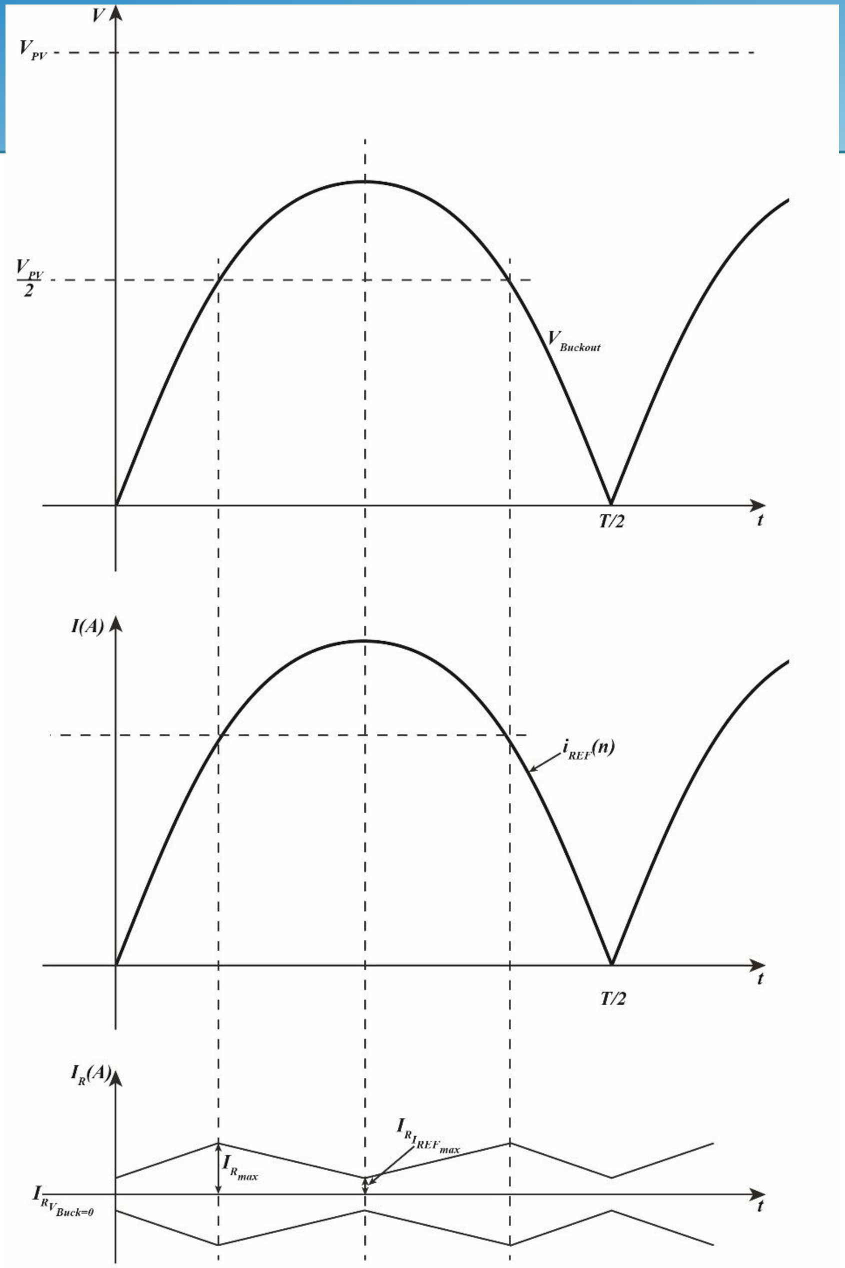


Figure 1 – Block diagram of the 300 W low cost micro-inverter


HFCS1 & LFCS1
CS1
CAL
Level Shift
x1,2,4 and 8
DAC8 6b
25 kHz, 50 kHz , 100 kHz or bypass
DAC0 10b
CMP00
IMATCH
PEAK
CMP01
IMATCH
TROUGH
DAC1 10b



$$I_{REF\,max} = \sqrt{2}\frac{P_{out}}{V_{Grid}}N_{T_1}$$

$$i_{REF}(n) = I_{REF\,max} sin\left(\frac{2\pi n}{256}\right) \text{ for } n = 0 \dots 255$$

$$I_{\text{DAC\_}peak1}(n) = i_{REF}(n) + I_{R_n}$$

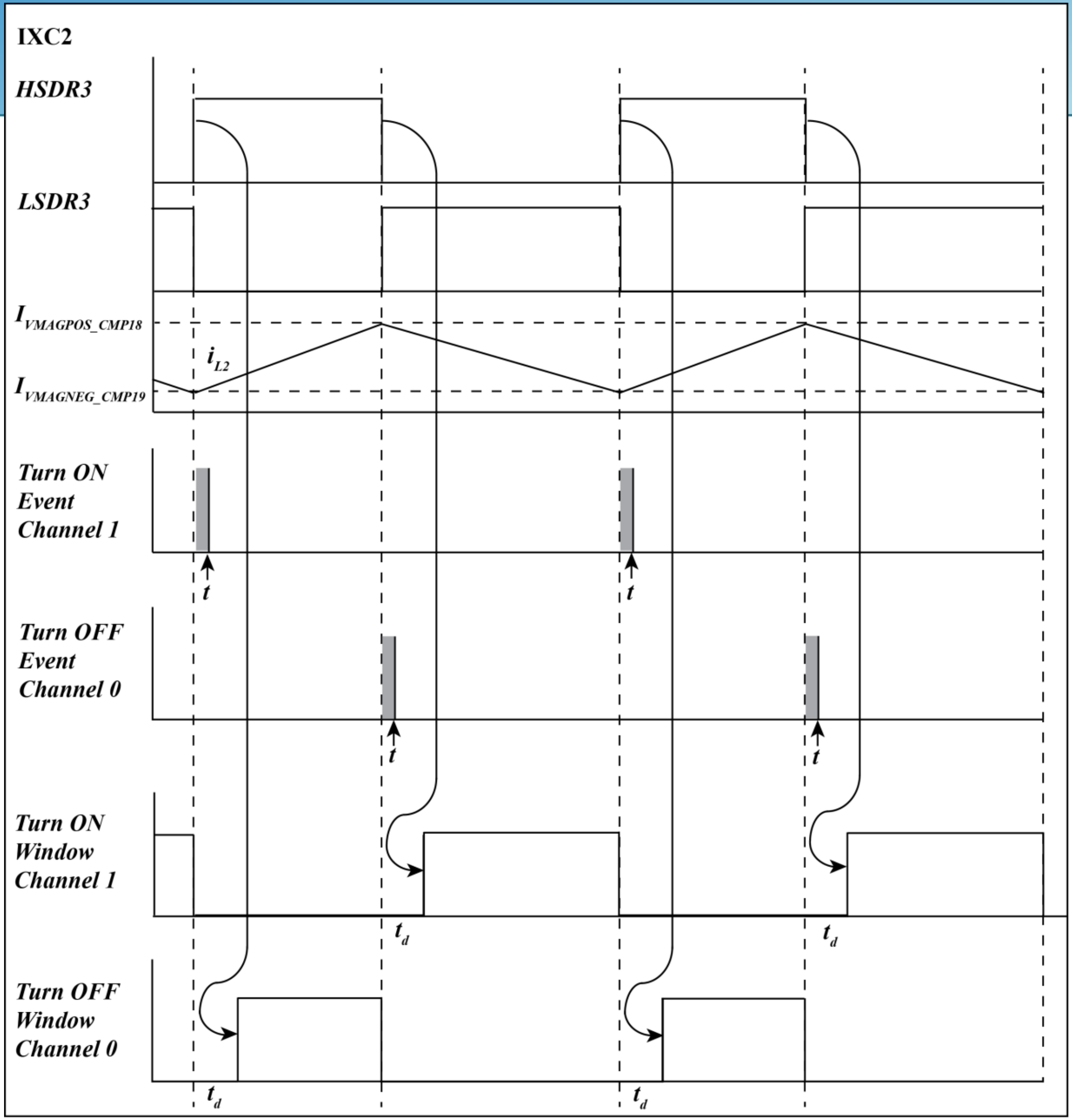
$$I_{DAC\_trough}(n) = i_{REF}(n) - I_{R_n}$$

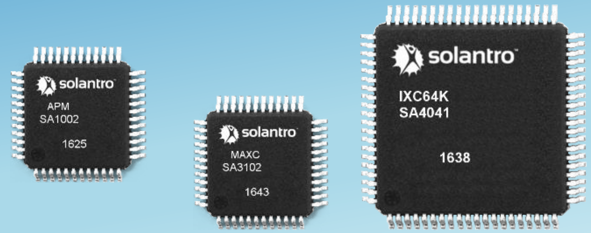
$$I_{R_n} = I_{R_{V_{Buck}=0}} + \frac{I_{R_{max}} - I_{R_{V_{Buck}=0}}}{64}\frac{n}{256f} \qquad \text{for } n = 1 \dots 64$$

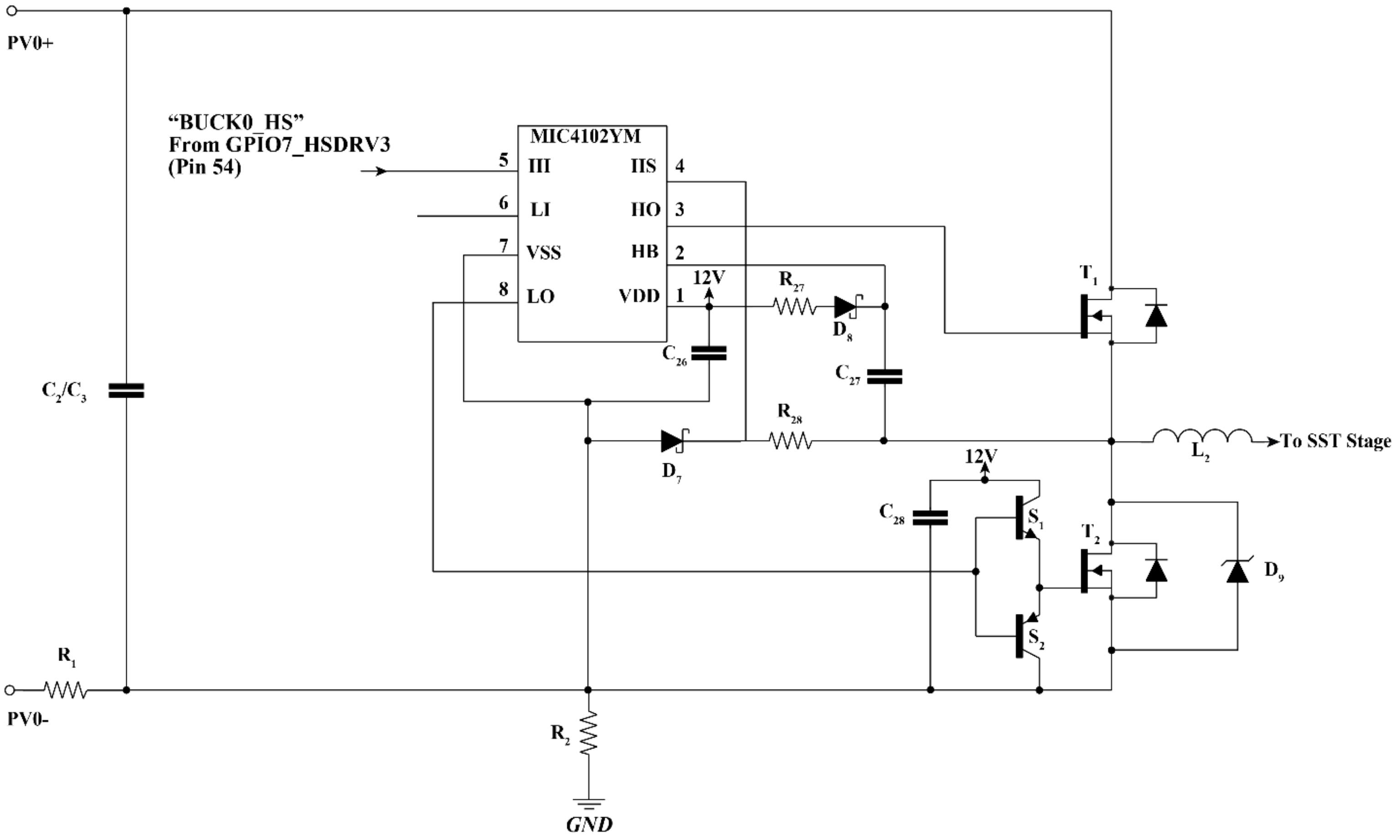
$$I_{R_n} = I_{R_{max}} + \frac{I_{R_{min}} - I_{R_{max}}}{64}\frac{n-64}{256f} \quad \text{for } n = 64 \dots 128$$

$I_{R_{max}}$, $I_{R_{min}}$, and $I_{R_{V_{Buck}=0}}$ are tuned to obtain maximum efficiency of the inverter.

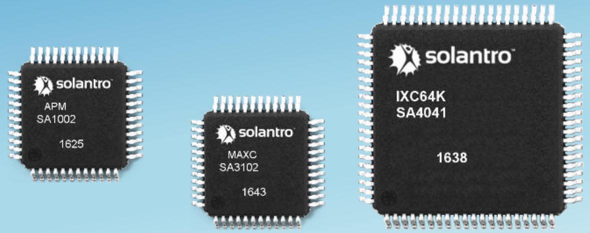

solantro
APM
SA1002
1625
solantro
MAXC
SA3102
1643
solantro
IXC64K
SA4041
1638

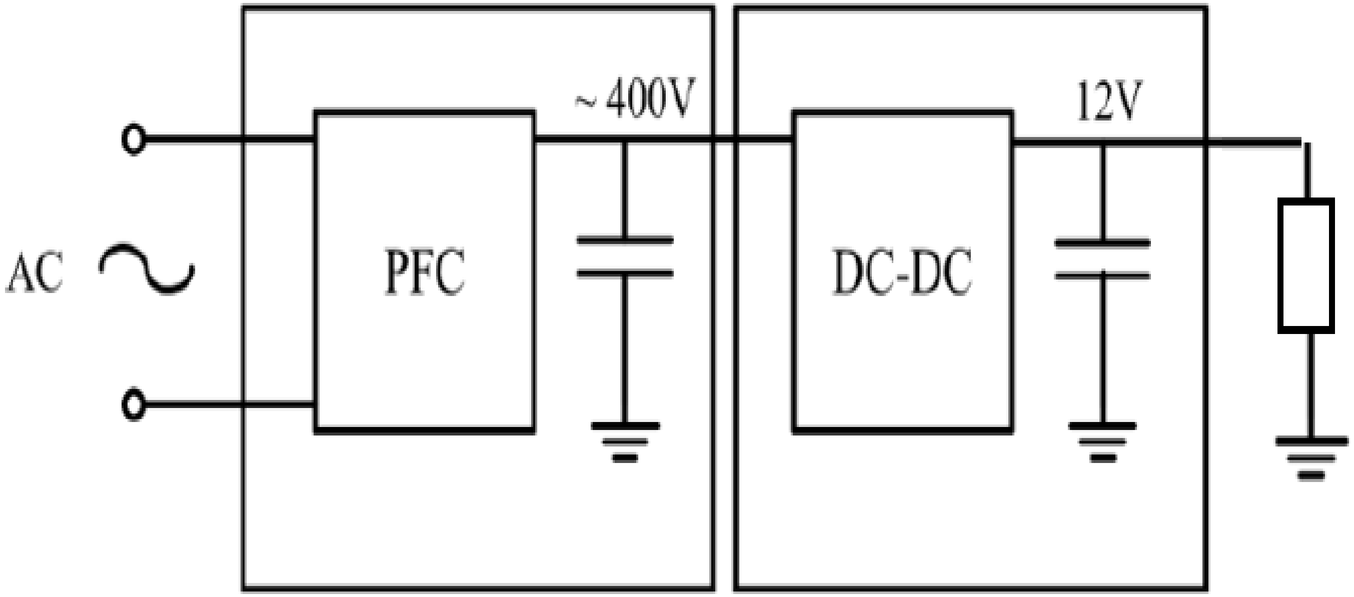

IXC2
HSDR3
LSDR3
$I_{VMAGPOS\_CMP18}$
i_{L2}
$I_{VMAGNEG\_CMP19}$
Turn ON Event Channel 1
t
t
Turn OFF Event Channel 0
t
t
Turn ON Window Channel 1
t_d
t_d
Turn OFF Window Channel 0
t_d
t_d


solantro
APM
SA1002
1625
solantro
MAXC
SA3102
1643
solantro
IXC64K
SA4041
1638


PV0+
“BUCK0_HS”
From GPIO7_HSDRV3
(Pin 54)
MIC4102YM
5
HI
6
LI
7
VSS
8
LO
HS
4
HO
3
HB
2
VDD
1
12V
R_{27}
D_8
C_{26}
C_{27}
T_1
C_2/C_3
R_{28}
D_7
L_2
To SST Stage
12V
C_{28}
S_1
T_2
D_9
S_2
R_1
PV0-
R_2
GND

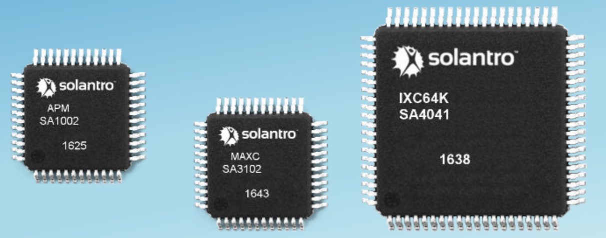
Power supply





The dement for PFC circuit is mainly driven by EN61000-3-2, ENERGY STAR® and 80 PLUS® standards.

PFC



Definition of thee power factor, *PF*, of an AC electrical power system

$$PF = \frac{P}{S}$$

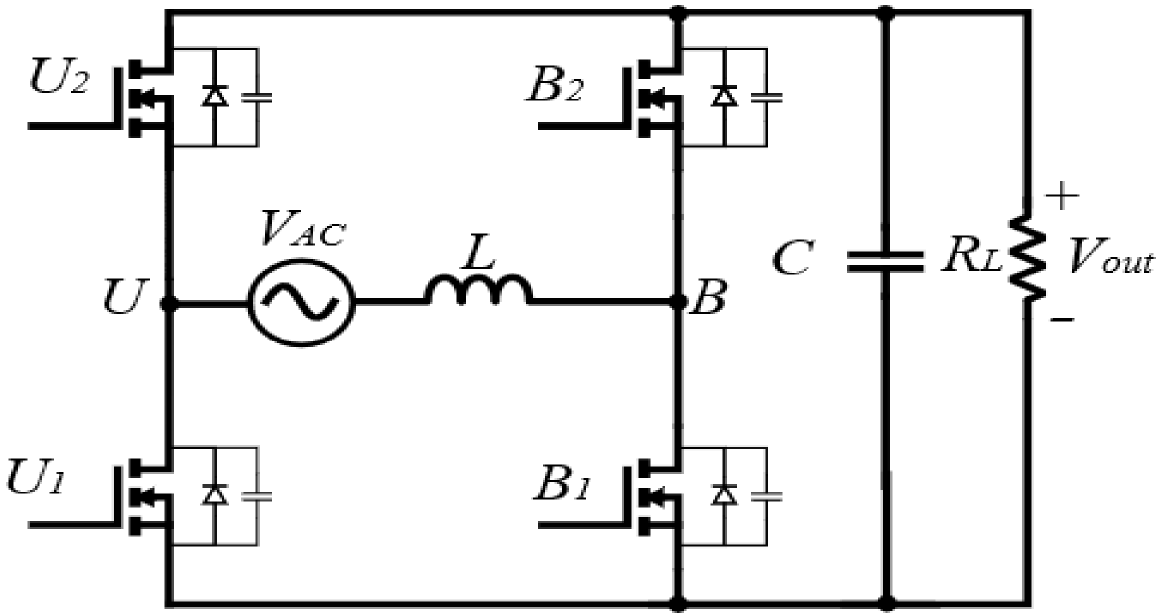
real power
apparent power

$$PF = Displacement\ Factor \times Distortion\ Factor$$

$$Displacement\ Factor = cos\varphi$$

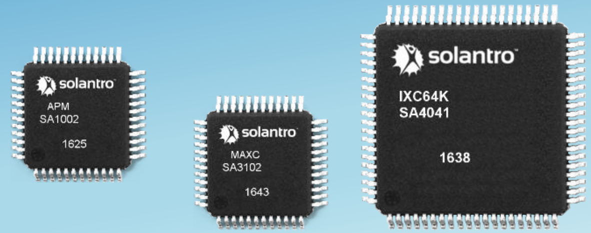
$$Distortion\ Factor = \frac{1}{\sqrt{1 + THD^2}}$$

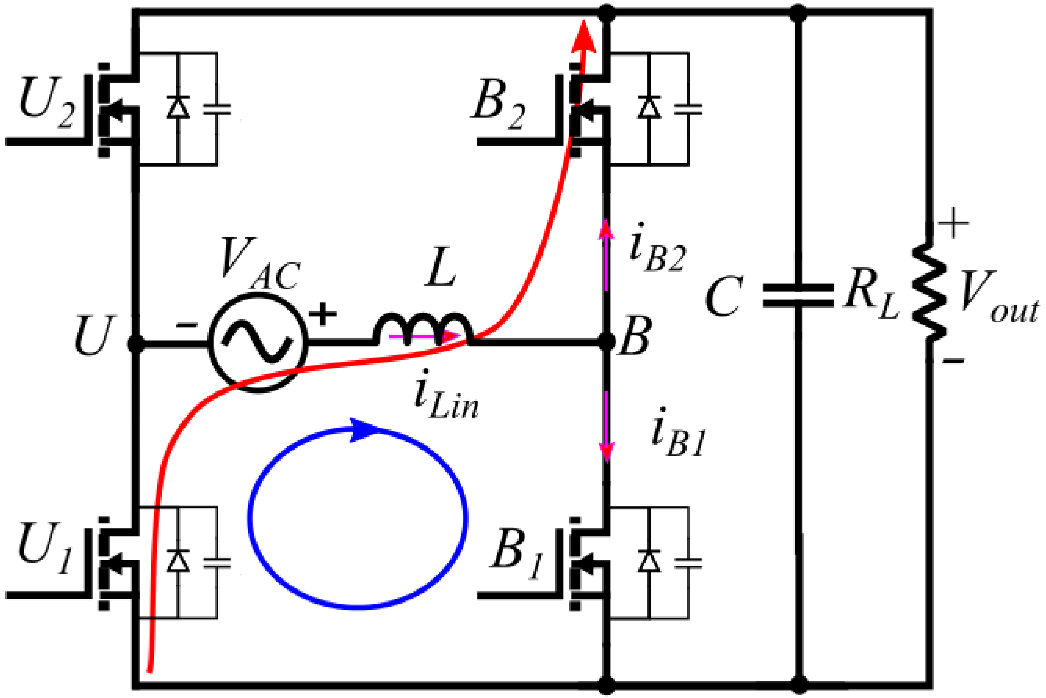
$$THD = \sqrt{\left(\frac{I_2}{I_1}\right)^2 + \left(\frac{I_3}{I_1}\right)^2 + \cdots}$$



Totem-pole bridgeless PFC converter.

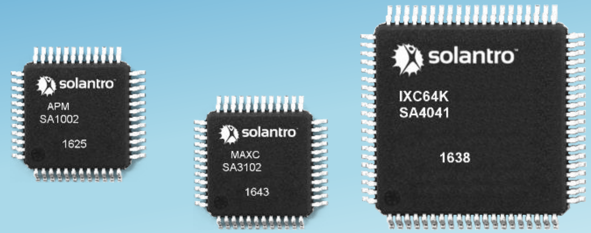
PFC

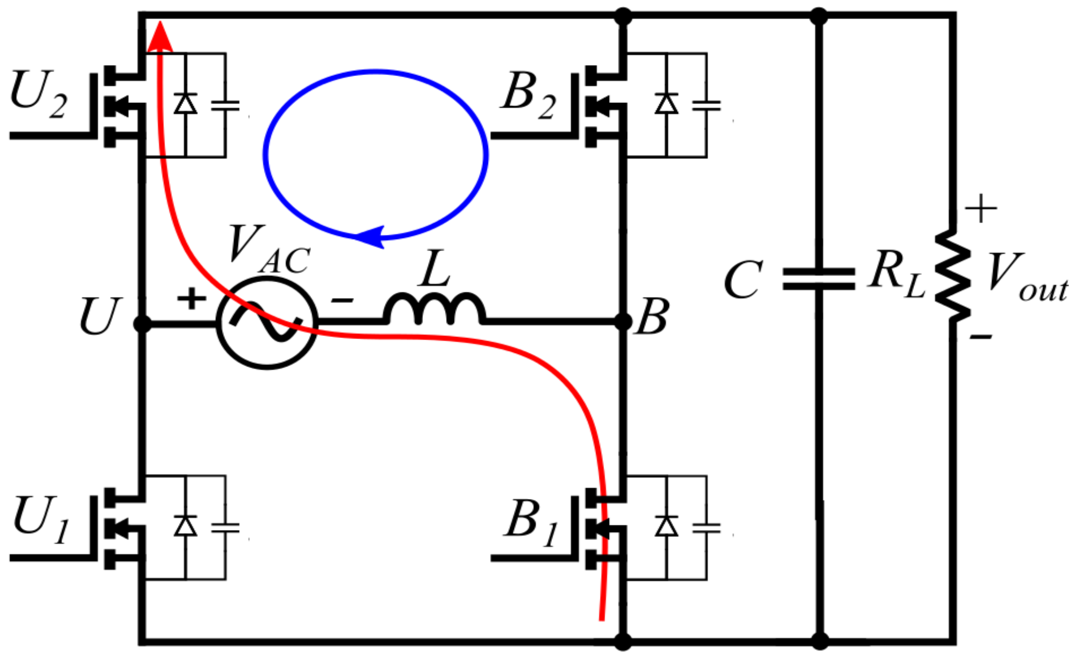




The positive half-line cycle equivalent boost circuit

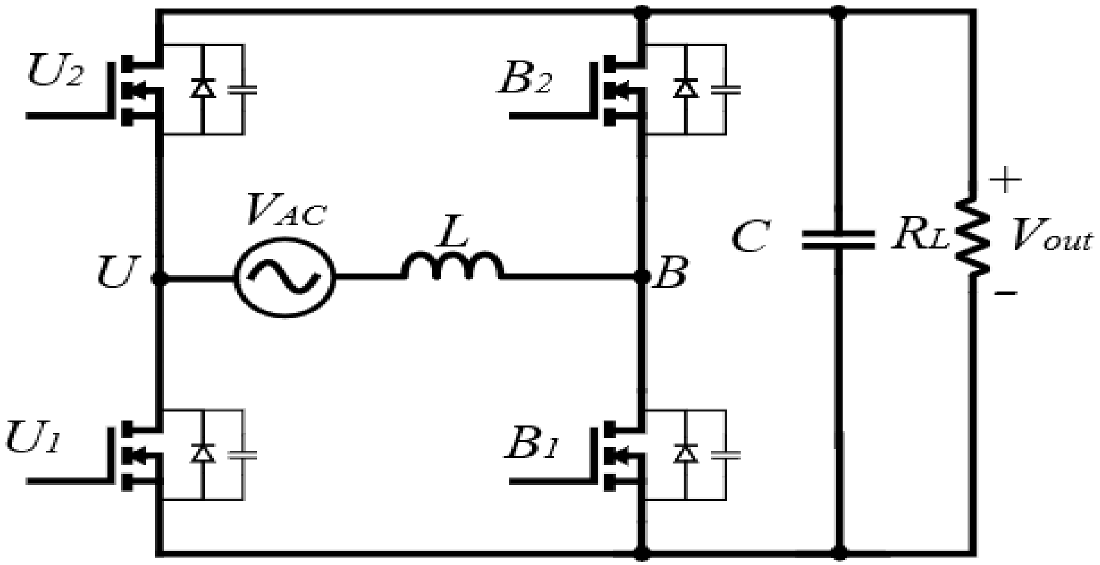
PFC





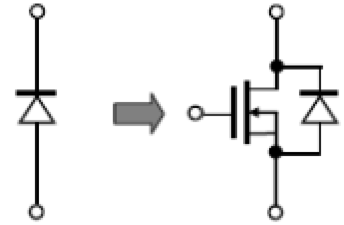
The negative half-line cycle equivalent boost circuit.

PFC



Totem-pole bridgeless PFC converter.

To improve the efficiency of the totem pole PFC synchronies rectification can be used.
The converter operates as follow.
Switch B_1 is *ON*, the current trough the inductor is rising.
When the inductor current reaches peak value, the switch B_1 is turned *OFF* and after some delay, the switch B_2 is turned *ON*, the current trough the inductor is decreasing and when it reaches the trough value and after another delay, the switch B_1 is turned *ON*.
During the two delays, the currents are passing through the switches intrinsic diodes and capacitors as it is explained above for no synchronous rectification.

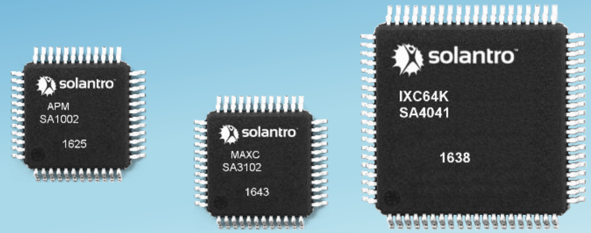


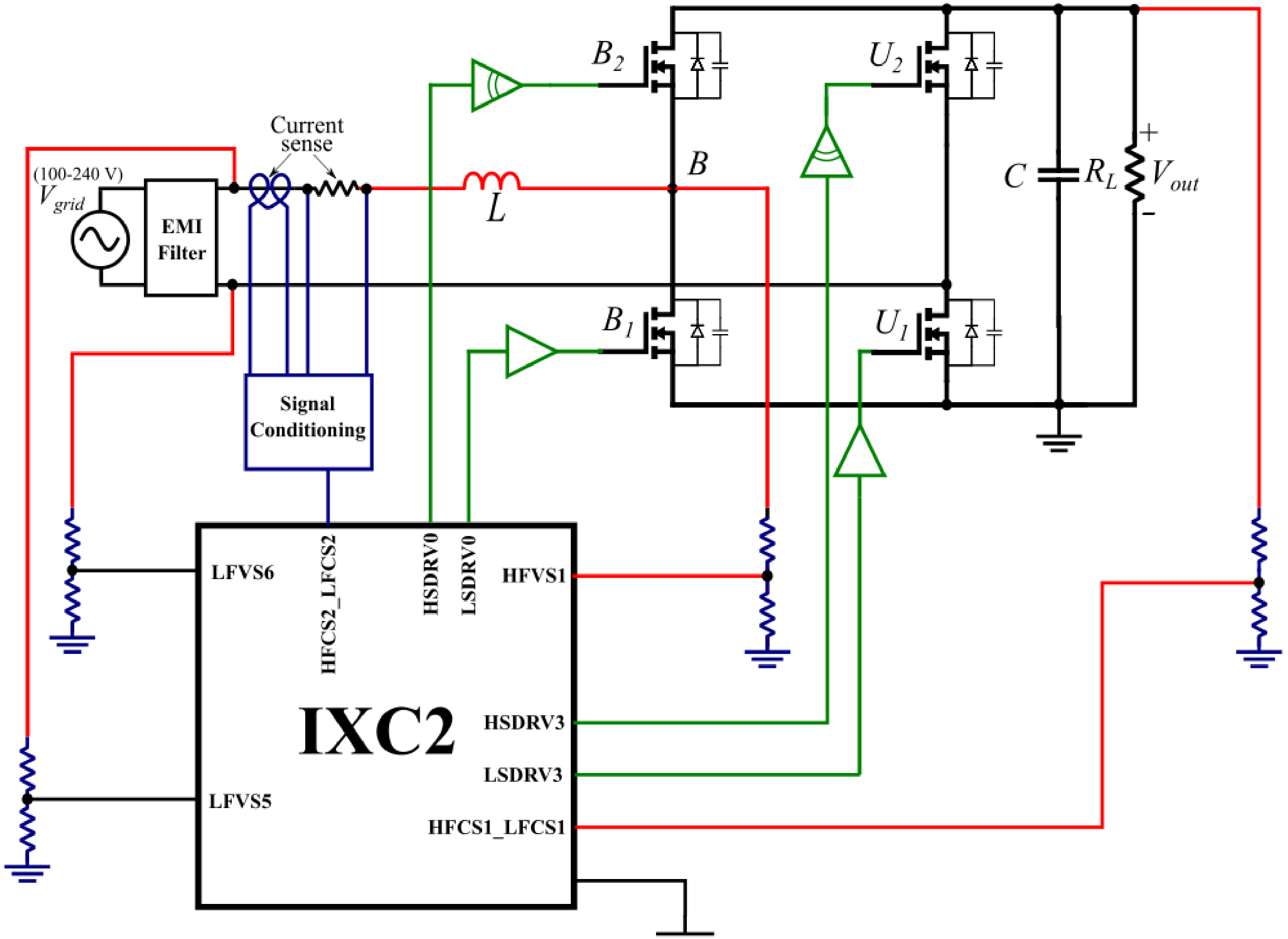
Dead time is necessary to avoid cross conduction!

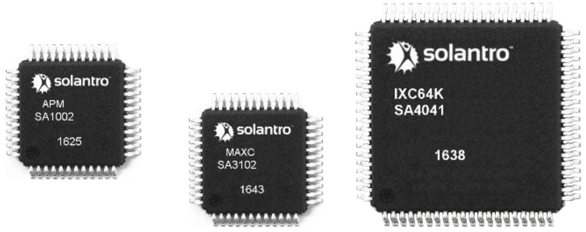
Using IXC2 event driven timers, the two delays can be changed dynamically during the operation and therefore the efficiency of the total pole PFC can be further improved.

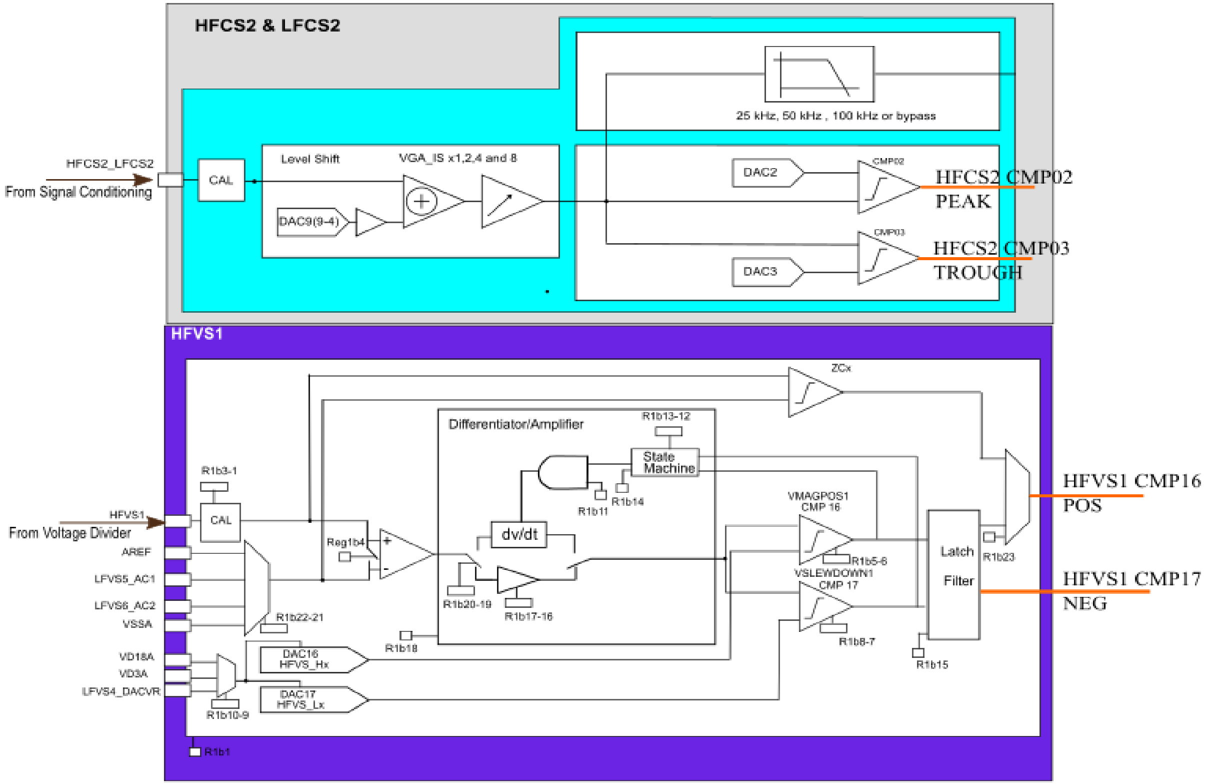
22

PFC

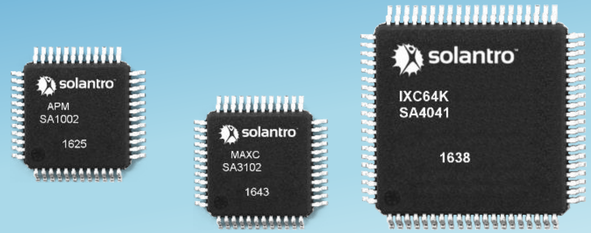

solantro
APM
SA1002
1625
solantro
MAXC
SA3102
1643
solantro
IXC64K
SA4041
1638

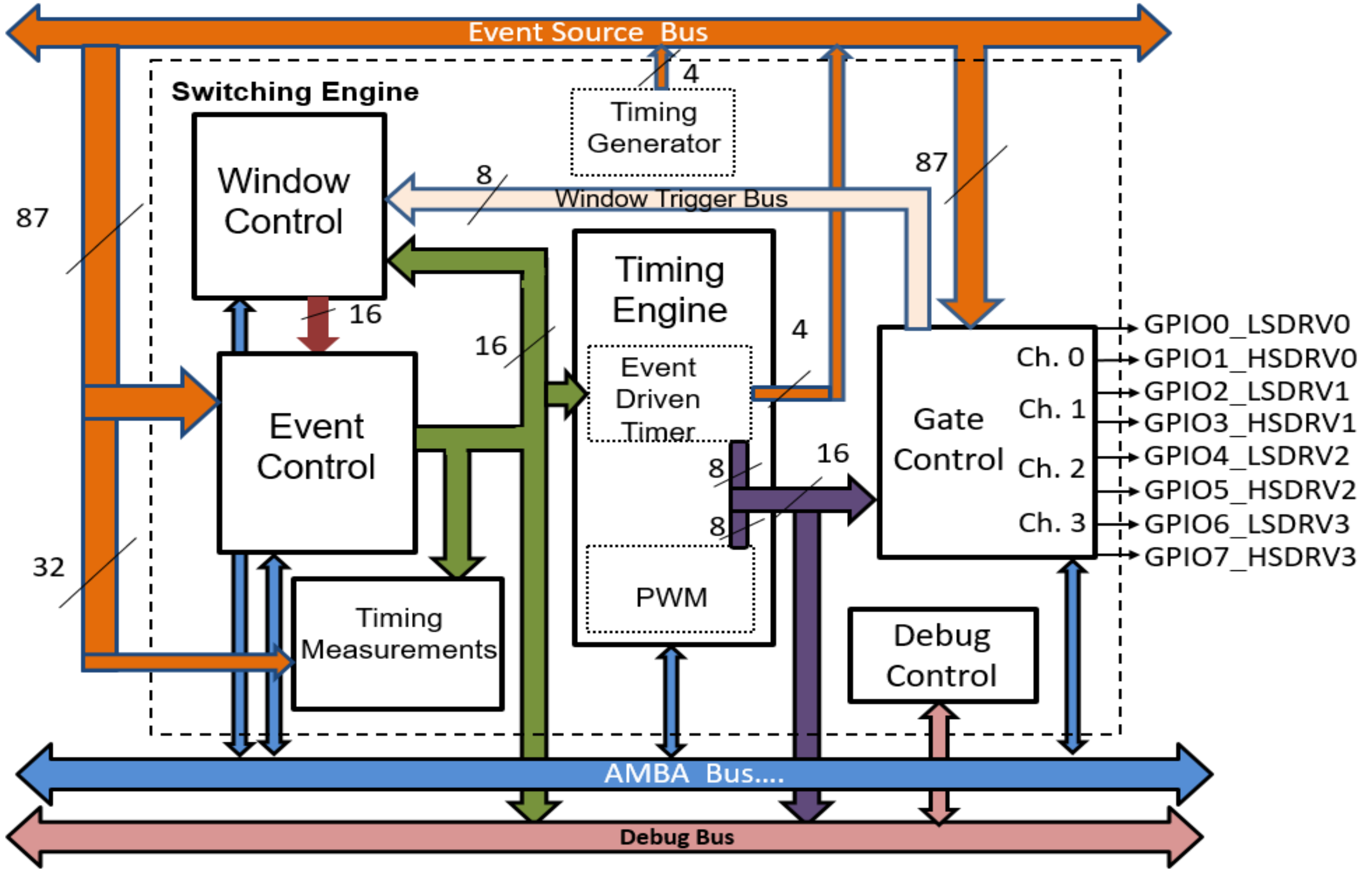

(100-240 V)
V_{grid}
EMI Filter
Current sense
Signal Conditioning
L
B
B_2
B_1
U_2
U_1
C
R_L
+
V_{out}
-
LFVS6
HFCS2_LFCS2
HSDRV0
LSDRV0
HFVS1
IXC2
HSDRV3
LSDRV3
LFVS5
HFCS1_LFCS1



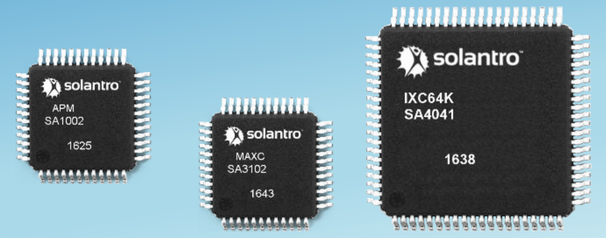


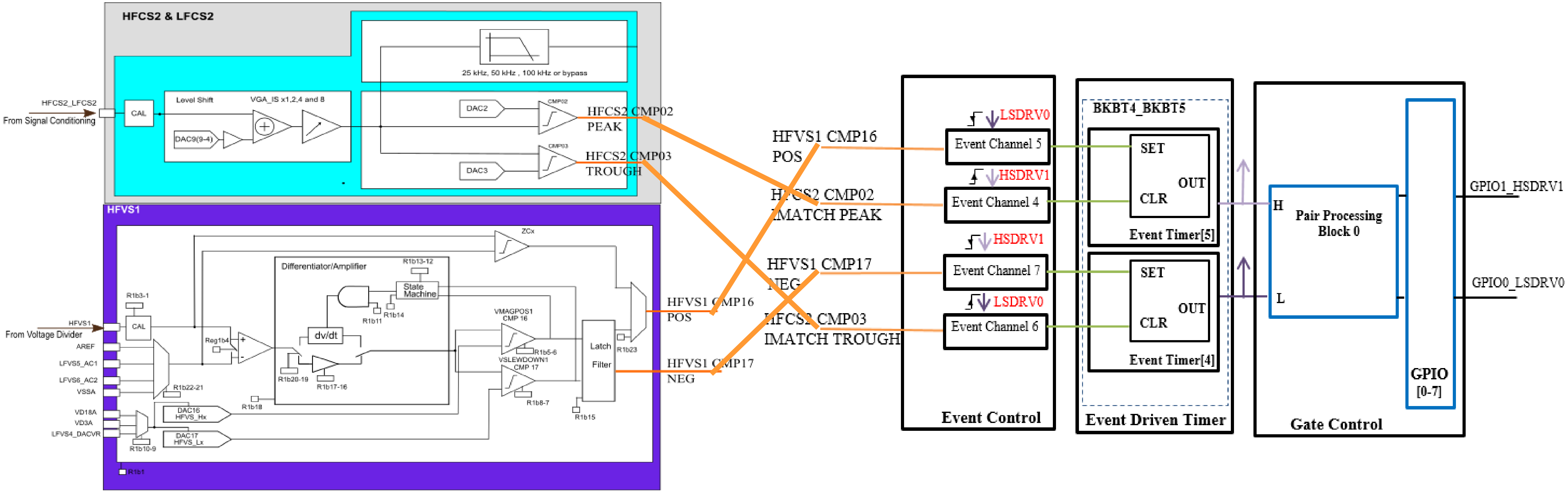
IXC2 HFCS2_LFCS2 and HFVS1 block diagrams





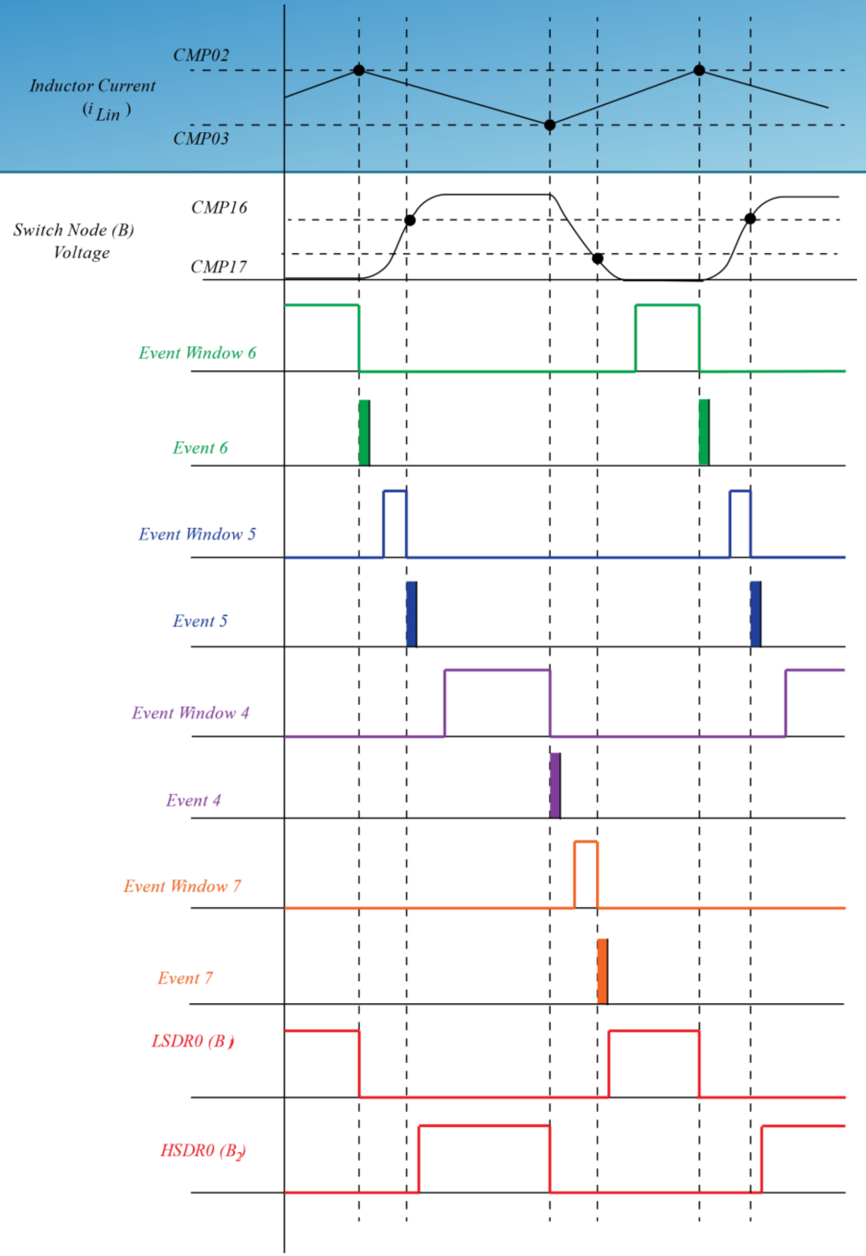
IXC2 Switching Engine

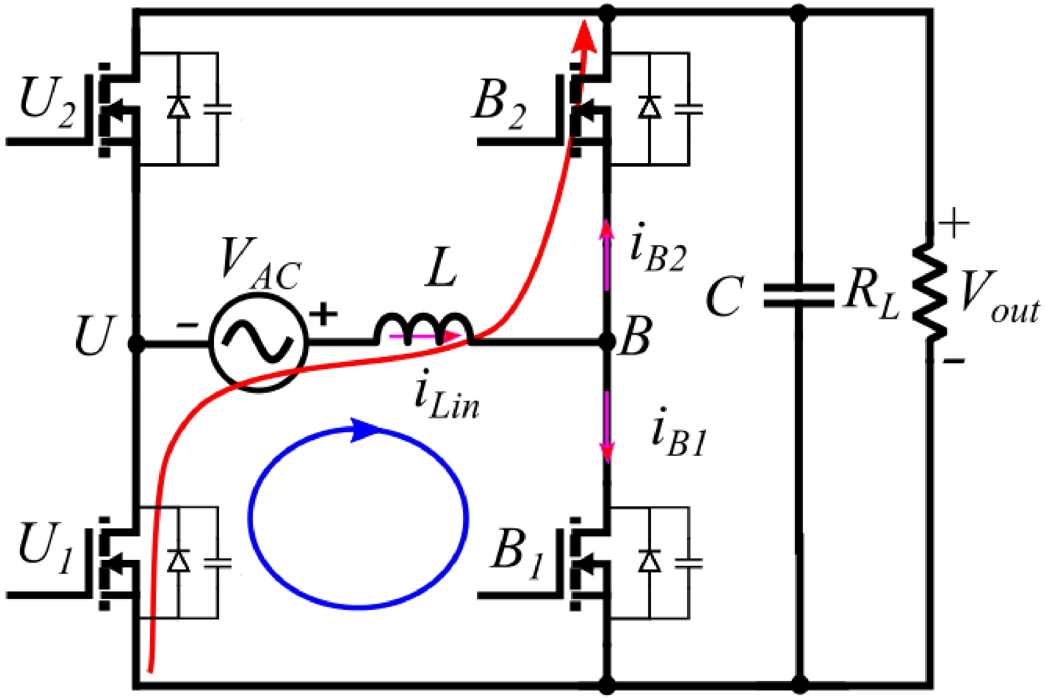




IXC2 Switching Engine configuration for Solantro Totem pole PFC

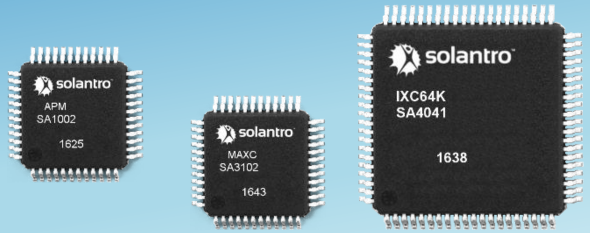
PFC

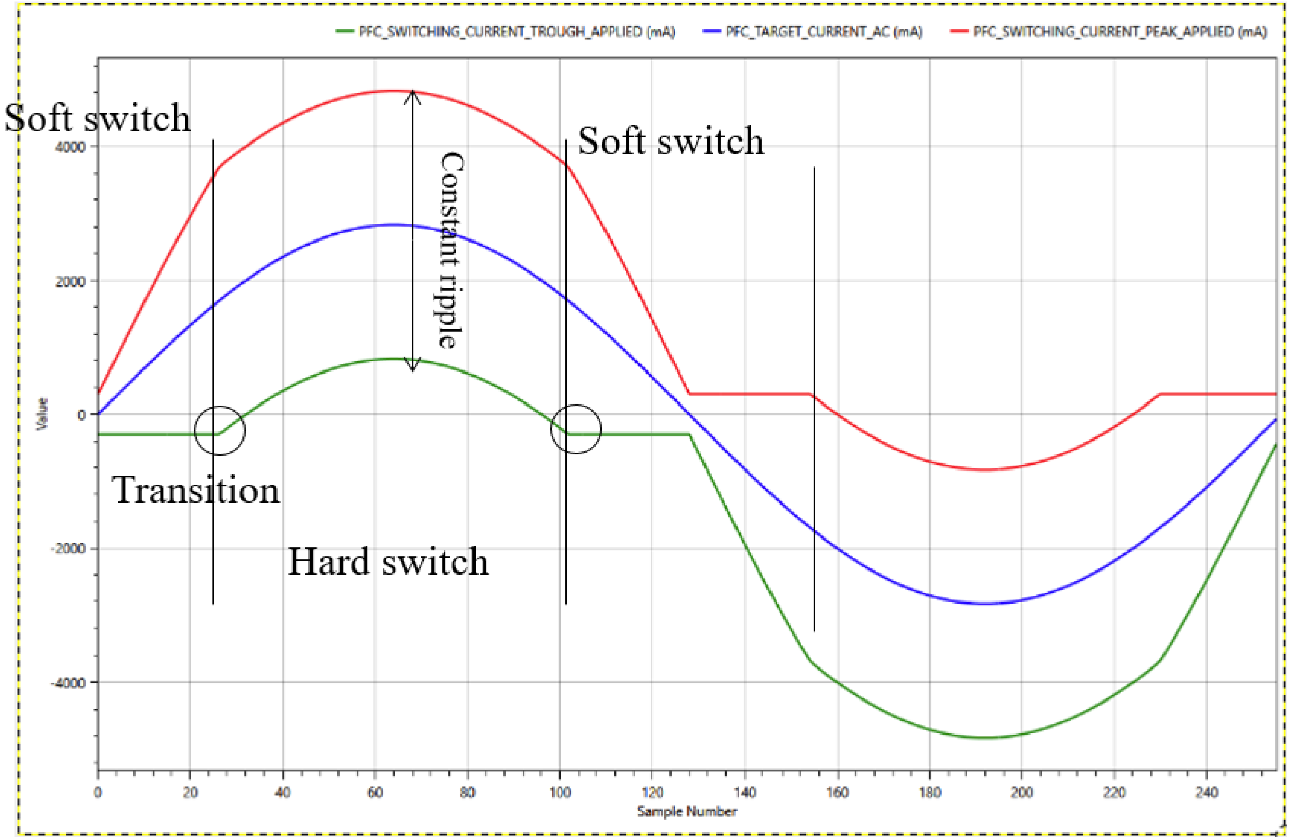




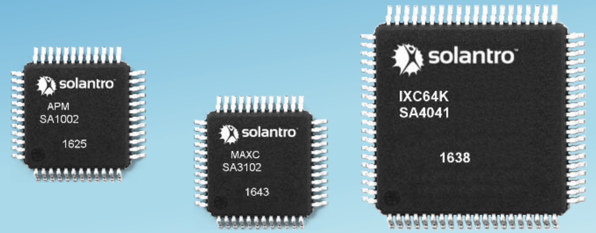
Timing diagram of the Solantro Totem pole PFC Boost 1.

PFC

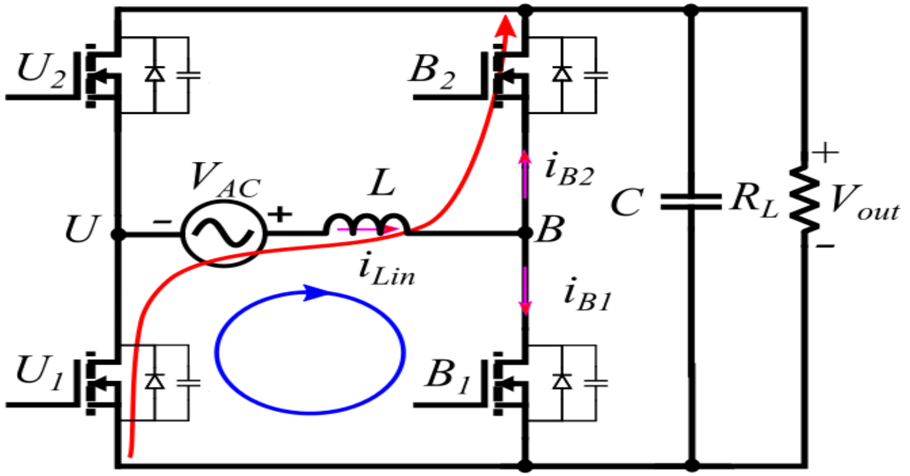

solantro
APM
SA1002
1625
solantro
MAXC
SA3102
1643
solantro
IXC64K
SA4041
1638

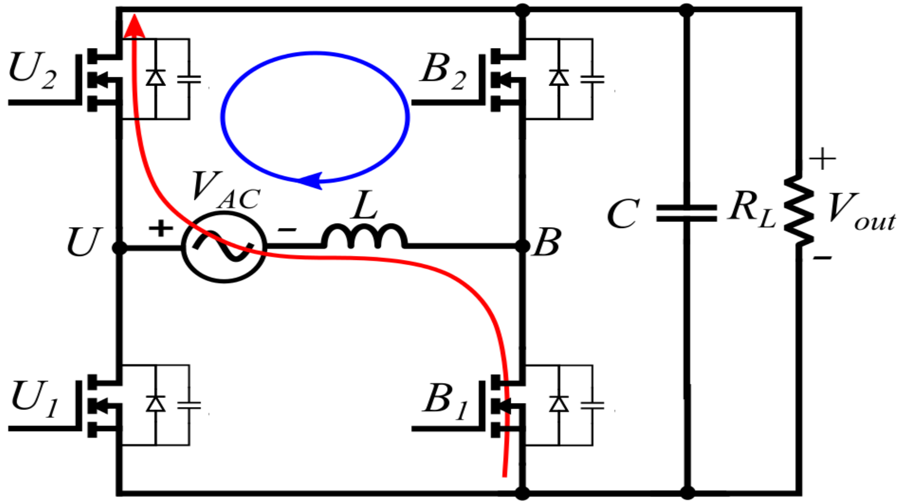

PFC_SWITCHING_CURRENT_TROUGH_APPLIED (mA)
PFC_TARGET_CURRENT_AC (mA)
PFC_SWITCHING_CURRENT_PEAK_APPLIED (mA)
Soft switch
Soft switch
Constant ripple
Transition
Hard switch
Value
4000
2000
0
-2000
-4000
0
20
40
60
80
100
120
140
160
180
200
220
240
Sample Number

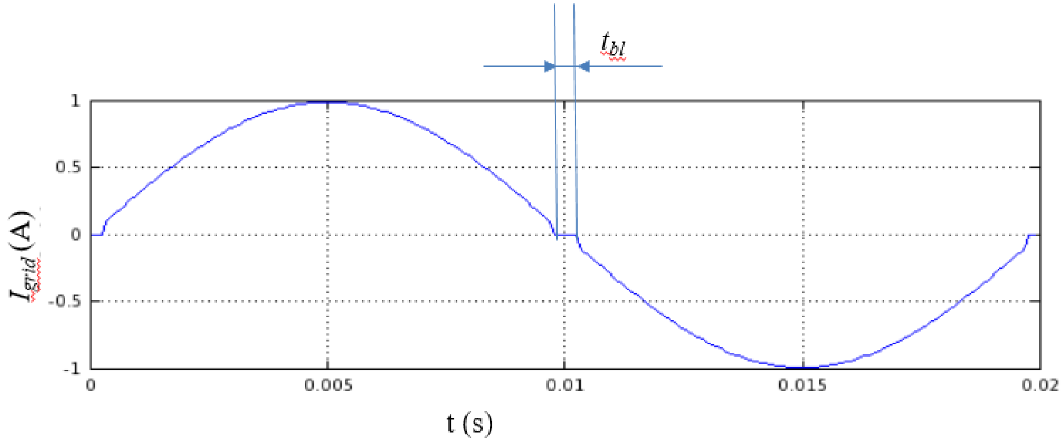
PFC



Totem Pole PFC hardware and control loop for the low frequency switches



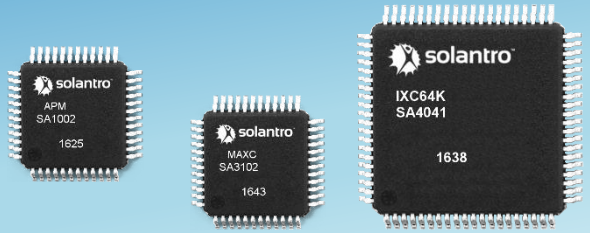




$$t_{bl_{min}} = n_{min}\Delta t$$

n_{min}	THD, %
2	0.43
4	0.97
6	1.62
8	2.37
10	3.21
12	4.13

$$V_{Grid} > V_{bl} \ \ and\ n \geq n_{bl}$$



IEEE Ottawa Section

pels

e-mail contacting: ottawapels@gmail.com

Thank you