Chapter 4 Solutions

1.

BLF/KHz	TRcal/us	DR
640	33.33	64/3
320	66.7	64/3
	25	8
160	133.3	64/3
	50	8
80	100	8

2. Solution (in hex)

(a) E2F0

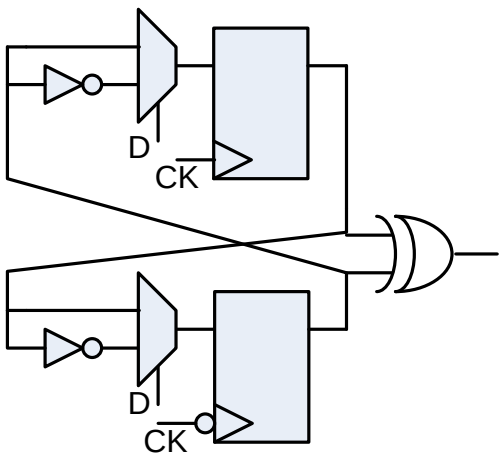
(b) CCAE

(c) 968F

(d) 78F6

3. To prevent a glitch at the clock net.

4.



5. The advantage is that the signal is shifted to BLF, immune to low-frequency noise. The disadvantage is that there is a lower data rate.

6.

Factors	Low power techniques
Power supply	Multi-Voltage tech., Sub-threshold tech.
Clock frequency	DET Flip-flop, Multi-clock
Activity probability	Clock-gating, operator isolation

7. Rounding methods:

[DISP]

Round to nearest; round towards zero; round down/floor; round up/ceil; round away from 0,…

[DISPX]

[FT]In the module to quantize and compute TRcal, RTcal and other parameters, the rounding method selected should guarantee that the mean quantization error introduced is zero, otherwise the BLF/decoding margin calculated will suffer a non-zero offset.

8.

[DISP]

$P_{tag,th}$ = -14 dBm = 40 μW. $\eta = P_{load} / P_{tag,th}$ = 12 / 40 = 30%.

[DISPX]

9. A feasible way to supply voltage generation is to have three different voltage levels of 0.65 V for Demod, clock generator and baseband, 0.85 V for RNG, POR generator, bias and regulator,

and finally 1.5 V for EEPROM.

10. M_b should be operating in the subthreshold region. During the turn-on period of this stage, the voltage drop V_{drop} on M_i equals to (in fact is a little larger than) V_{th} - V_{GSb}, where V_{th} is the threshold voltage and V_{GSb} is the gate-source voltage of M_b. V_{drop} needs to be close to zero to reduce the power loss on this stage. On the other hand, V_{GSb} must be smaller than V_{th} to reduce the reverse leakage current. Therefore, M_b operates in the subthreshold region.

11. In the tag system, the duty cycle of the fast clock may not be precisely equal to 50%. For example, if we use a D flip-flop, assuming the duty cycle of fast clock is 40%, the probabilities of 0 sampling and 1 sampling equal to $P(0) = 0.6$, $P(1) = 0.4$, respectively. However, T flip-flop does not have such problems. The output probability of a T-flip-flop equals

[DISP]

$$P_{n+1}(0) = P(0)P_n(0) + P(1)P_n(1) \tag{4.1}$$

$$P_{n+1}(1) = P(0)P_n(1) + P(1)P_n(0) \tag{4.2}$$

[DISPX]

[FT]where $P_n(0)$ and $P_n(1)$ are the n^{th} sample probabilities for 0 and 1, $P_{n+1}(0)$ and $P_{n+1}(1)$ are the $(n+1)^{th}$ sample probabilities for 0 and 1. By (4.1) and(4.2), we can have

[DISP]

$$\begin{aligned} P_{n+1}(0) = &\frac{1}{2}\left[\left(P(0)+P(1)\right)^n + \left(P(0)-P(1)\right)^n \right] P_1(0) \\ &+ \frac{1}{2}\left[\left(P(0)+P(1)\right)^n - \left(P(0)-P(1)\right)^n \right] P_1(1) \end{aligned} \tag{4.3}$$

$$\begin{aligned} P_{n+1}(1) = &\frac{1}{2}\left[\left(P(0)+P(1)\right)^n - \left(P(0)-P(1)\right)^n \right] P_1(0) \\ &+ \frac{1}{2}\left[\left(P(0)+P(1)\right)^n + \left(P(0)-P(1)\right)^n \right] P_1(1) \end{aligned} \tag{4.4}$$

[DISPX]

[FT[Since $P_n(0) + P_n(1) = 1$ and $0 < |P_n(0) + P_n(1)| < 1$, the possibilities for 0 sampling and 1 sampling in a long run are

[DISP]

$$\lim_{n\to\infty} P_{n+1}(0) = \frac{1}{2}\ P_1(0) + P_1(1)\ = 0.5 \tag{4.5}$$

$$\lim_{n\to\infty} P_{n+1}(1) = \frac{1}{2}\ P_1(0) + P_1(1)\ = 0.5 \tag{4.6}$$

[DISPX]