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Photonic analog-to-digital conversion using multiple comparators and Mach-Zehnder modulators with identical half-wave voltages

Shuna Yang [a], Zhiguo Shi [a,*], Hao Chi [a], Xianmin Zhang [a], Shilie Zheng [a], Xiaofeng Jin [a], Jianping Yao [a,b]

[a] Department of Information and Electronic Engineering, Zhejiang University, Hangzhou 310027, China
[b] Microwave Photonics Research Laboratory, School of Information Technology and Engineering, University of Ottawa, Ottawa, Canada K1N 6N5

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ABSTRACT

A novel photonic analog-to-digital conversion scheme using Mach-Zehnder modulators (MZMs) with identical half-wave voltages and multiple comparators with improved bit resolution is proposed and demonstrated. Compared with the scheme using MZMs with geometrically scaled half-wave voltages, the proposed scheme has the advantage of using MZMs with identical half-wave voltages which simplify significantly the implementation. The bit resolution is improved based on the use of multiple comparators in each MZM channel, with the digital coding realized based on the symmetrical number system theory. A proof-of-concept experiment is implemented. An analog-to-digital converter with a 4-bit resolution using two MZMs and nine comparators is demonstrated.

1. Introduction

Analog-to-digital converter (ADC) realized in the optical domain has been an attractive research topic for many years thanks to the unique ability of ultra high speed sampling offered by the state-of-the-art optical mode-locked lasers. By now, numerous approaches to realizing optical sampling and optical quantization have been proposed and demonstrated [1]. A well-known architecture for photonic ADC is the scheme proposed by Taylor, in which an array of parallel Mach-Zehnder modulators (MZMs) are used [2], with geometrically scaled half-wave voltages (V_π) realized by controlling the electrode lengths of the MZMs. The major limitation related to Taylor's scheme is that the V_π of the MZM at the least significant bit (LSB) should be very low, which is difficult to realize using current waveguide technology. To avoid using MZMs with very low V_π, an approach employing cascaded MZMs with identical V_π was proposed [3,4].

Instead of using an array of MZMs, a photonic ADC can also be realized using a single modulator. Recently, Stigwall et al. proposed a photonic ADC with a free-space interferometric structure in which a phase modulator is incorporated in one arm of the interferometer [5,6]. By placing an array of photodetectors (PDs) at the specific locations of the diffraction pattern generated at the output of the interferometer, digital data in the form of a linear binary code are generated. A similar scheme was recently demonstrated by Li et al., where the interferometric structure was realized based on a fiber-optic platform, which makes the system more compact [7]. More recently, we proposed a new scheme of photonic ADC using MZMs with identical half-wave voltages [8]. The quantization and digital coding are achieved by properly biasing the MZMs, with each MZM being connected to a comparator with the threshold setting at half of the maximum voltage. A binary code representing the input analog signal is generated. Compared with the Taylor's scheme, the bit resolution achieved in [8] is smaller. For an ADC using n MZMs, the bit resolution is $\log_2(2n)$; while in the Taylor's scheme, the number of bit resolution *equals to* the number of MZM*s* employed.

To increase the bit resolution without increasing the number of MZMs, Pace et al. proposed to use multiple comparators with each having a different threshold level [9]. The digital coding is achieved based on the theory of symmetrical number system (SNS). It is shown that by using multiple comparators with the SNS encoding, a bit resolution greater than one for each channel (corresponding to a MZM) can be obtained. To avoid the ambiguity problem, the MZMs should have a small difference in V_π [9]. Therefore, the difficulty in implementing the MZMs with different V_π still exists.

In this paper, a novel scheme for photonic ADC using an array of MZMs with identical V_π and multiple comparators for each channel is presented. By setting the threshold values of the comparators based on the SNS technique, an increased bit resolution is obtained. To avoid the ambiguity problem, the MZMs are biased at different bias points. This is the key advantage compared with the approach by Pace et al. [9], where the MZMs are with different V_π, which complicated significantly the system implementation. A photonic ADC scheme with a 4-bit resolution using two MZMs and nine

* Corresponding author. Tel.: +86 571 87953855.
E-mail addresses: shizg@zju.edu.cn (Z. Shi), chihao@zju.edu.cn (H. Chi), zhangxm@zju.edu.cn (X. Zhang), zhengsl@zju.edu.cn (S. Zheng), jpyao@site.uottawa.ca (J. Yao).

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comparators is demonstrated in a proof-of-concept experiment. The presented experimental results verify the effectiveness of the proposed approach.

2. Operation principle

The schematic diagram of the proposed scheme is shown in Fig. 1. It is an n channel ADC consisting of an array of n MZMs with identical V_π and multiple comparators for each channel. The MZMs are properly biased. The input analog signal to be digitized is applied to the MZMs via the RF ports. A mode-locked laser is used to provide ultra-short pulse train. The output signal from each MZM is split into multiple channels by an optical splitter with each channel connected to a PD to perform optical-to-electrical conversion. The electrical signal is then applied to the comparator with a preset threshold to get a quantized output in the form of a thermometer code [9]. A combining logic is employed to convert the thermometer code to a required digital code.

The intensity of the output signal from a MZM is associated with the input analog signal and the bias voltage which is expressed as

$$I_0(t) = \frac{I_i}{2}\{1 + \cos[\varphi_s(t) + \varphi_b]\}, \quad (1)$$

where I_i is the input optical intensity, $\varphi_s(t) = \pi V_s(t)/V_\pi$ is the phase shift induced by the applied RF signal $V_S(t)$, and $\varphi_b = \pi V_b/V_\pi$ is the phase shift induced by the applied bias voltage V_b. To get a uniform quantization, the MZMs should be biased such that the transfer functions are phase-shifted uniformly.

The coding scheme is based on the theory of SNS that utilizes a positive integer modulus m [9,10]. For a given m, m comparators are required for each MZM. With the output signal given by Eq. (1), the preset threshold values for the comparators are given by

$$T_j = \cos^2\left[\frac{\pi}{2mV_j} + \frac{\pi}{2} - \frac{\pi}{4m}\right], \quad (2)$$

where $V_j \in \{1, 1/2, 1/3, 1/4, \ldots, 1/(m-1), 1/m\}$. For each comparator, the output is '1' if the input signal is greater than the preset threshold and the output is '0' if the input signal is smaller than the preset threshold. The number of output '1' in all channels can be used to uniquely denote the input signal intensity. The coding based on the number of output '1' is called a thermometer code [9].

For an n-channel ADC shown in Fig. 1, n MZMs and $n \times m$ comparators are required, and the bias phase shift applied to each MZM should be

$$\varphi_b^j = -\frac{j\pi}{m(n-1)} - \frac{\pi}{16} \quad (j = 0, 1, 2, \ldots, n-1). \quad (3)$$

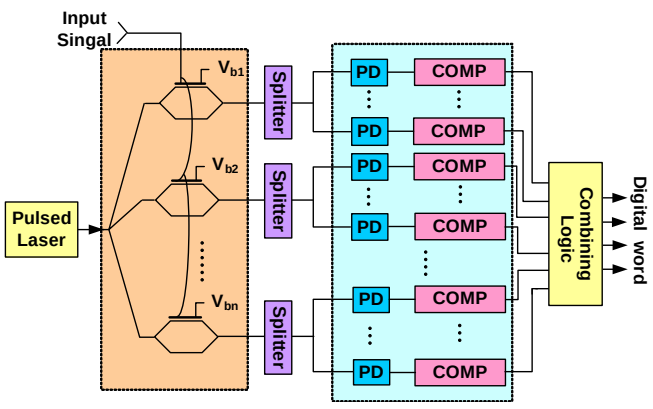


Fig. 1. An n-channel ADC using MZMs with identical half-wave voltages and multiple comparators (PD: photodetector; COMP: comparator).

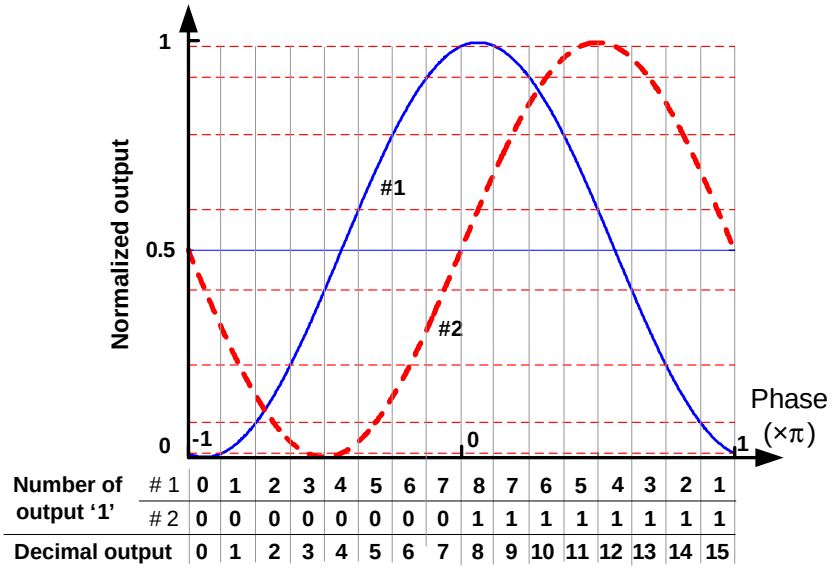
The number of quantization levels is $M = 2m(n-1)$, and the bit resolution is given by $N_R = \log_2[2m(n-1)]$.

It can be simply deduced that to add $2m$ more quantization levels it is required to add one more channel consisting of one MZM and m comparators. To reduce the complexity of the system, the scheme shown in Fig. 1 can be modified as follows. In the system, one of the MZM channels with m comparators can be simplified to have only one comparator, with the threshold set at half of the full scale. Note that this one-threshold channel should have a bias phase shift $\varphi_b = -\pi/2$, while the bias phase shifts of other channels are still set according to Eq. (3). *To ensure correct and unique* coding, the set of the bias phase shift value should be $\varphi_b = -\pi/2$, which makes the normalized output I_0 in the range of $0 < I_0 < 0.5$ for the input signal phase shift range *of* $-\pi < \varphi_s < 0$ and $0.5 < I_0 < 1$ for $0 < \varphi_s < \pi$, which can be clearly understood in the following example. The number of the comparators in system can be reduced from 16 to 9 and the thermometer code obtained in this scheme can still uniquely denote the intensity of the input signal, while keeping the original bit resolution. Then the number of the comparators required in the system is reduced by m-1.

To demonstrate the concept more clearly, a simple example with an ADC having a resolution $N_R = 4$ and $n = 2$, $m = 8$ is considered. The first channel has 8 comparators with the threshold values [0.0096 0.0843 0.2222 0.4025 0.5975 0.7778 0.9157 0.9904] determined by Eq. (2) and the second channel has one comparator with a threshold set at half of the full scale. The bias phase shifts of the two channels are $-\pi/16$ and $-\pi/2$, respectively. Fig. 2 shows the transfer functions of the two MZMs, where the horizontal axis is the phase shift induced by input RF signal and the vertical axis denotes the normalized intensity of the output optical signal. In the figure, the eight thresholds for channel 1 are denoted by horizontal dashed lines and the one threshold for channel 2 is denoted by the horizontal solid line. For each phase shift value induced by the input RF signal, the number of output '1' for each channel can be calculated by comparing the signal intensity with the preset thresholds. The output code representing the number of output '1' is just the thermometer code. The combination of the outputs of the two channels, i.e., the thermometer codes, can be used to uniquely denote the input signal intensity, which is shown in Fig. 2. Then the thermometer codes obtained are sent to a combination logic circuit, to convert the thermometer code to a required digital code, such as a binary code or a Gray code. The combination logic can be designed using the Karnaugh map [11]. As shown in Fig. 2, the combination of the two thermometer codes uniquely represent the decimal values from 0 to 15, which means the number of quantization levels is 16 and the bit resolution is 4.

3. Results and discussion

A proof-of-concept experiment with a 4-bit ADC is performed to verify the proposed scheme. The experimental setup is shown in Fig. 3. Due to the lack of a pulsed laser, a continuous-wave (CW) LD is used in our proof-of-concept experiment. The sampling process is implemented in an off-line mode *with a* computer program *being* used to implement the functions of off-line sampling and data processing. A CW laser diode (Yokogawa AQ2201) operating at 1550 nm is used as a single mode optical source. The input optical power is 5 dBm. A 20-GHz JDS-Uniphase MZM driven by a 4-GHz sinusoidal signal with power *of* 18 dBm generated by a signal generator (Agilent E8254A) is applied to the MZM via the RF port. A polarization controller (PC) is used to minimize the polarization-dependent loss in the MZM. A 45-GHz PD (New Focus 1104) is used to implement the optical-to-electrical conversion. A digital sampling oscilloscope (Agilent DCA 86100C) is used to capture the temporal waveforms, which is triggered by the signal generator.



Number of output '1'	# 1	0	1	2	3	4	5	6	7	8	7	6	5	4	3	2	1
	# 2	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Decimal output		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Fig. 2. Transfer functions of the MZMs (#1: $\varphi_b = -\pi/16$, #2: $\varphi_b = -\pi/2$). The thermometer codes and their corresponding decimal outputs are also shown.

The half-wave voltage V_π of the MZM is 9.2 V. The captured waveforms corresponding to different channels are processed in the *computer* in which the functions of sampling and coding are implemented.

In the experiment, the bias phase shift at the MZM is controlled by adjusting the applied bias voltage, with the waveforms measured for the bias voltages of $V_{b1} = -V_\pi/16$ and $V_{b2} = -V_\pi/2$. The recorded 2 traces (without averaging) that correspond to the two bias phase shifts are shown in Fig. 4a. We then sample the recorded signals in a program with a fixed time interval, to get discrete intensity data. Then, the operation of quantization and coding is performed by comparing the discrete data with the preset thresholds. The eight thresholds for the first channel are 0.0180, 0.0167, 0.0158, 0.0118, 0.0089, 0.0054, and 0.0030 mV; and the one-threshold for the second channel is 0.0116 mV. Then the coding process as depicted in Fig. 2 is implemented in the program. The results of the digitized signal and the fitted waveform are shown in Fig. 4b. Fig. 4c shows the errors between the quantized and the fitted signals. Based on the errors, the digital signal-to-noise ratio (dSNR) is estimated to be around 215 (or 23.3 dB). Therefore, the effective number of bits (ENOB) of the ADC is estimated to be around 3.6 according to [1]

$$\mathrm{ENOB} = \frac{\mathrm{dSNR(dB)} - 1.76}{6.02}. \tag{4}$$

Since the ideal resolution is 4 bits, a deviation from the ideal case is thus 0.4 bits. This degradation is owing to the noise in the system, including the relative intensity noise of the laser source, the shot noise and the thermal noise of the PD, and the instrument noise.

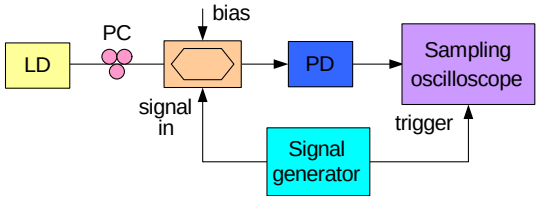


Fig. 3. Experimental setup (LD: laser diode, PC: polarization controller, PD: photodetector).

Since in our experiment, the sampling process is realized by software emulation, in which *an* ideal sampling, i.e., no sampling time jitter, is considered. Note that the deviation in the sampling time originated from the pulsing temporal jitter in a mode-locked

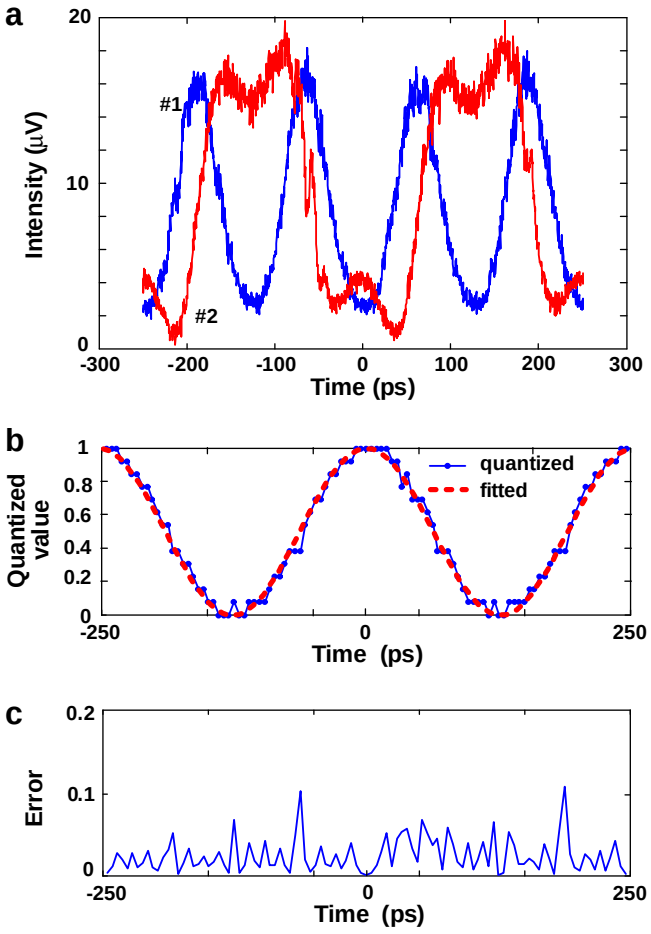


Fig. 4. Experiment results. (a) The measured two waveforms corresponding to two bias phase shifts (#1: $\varphi_b = -\pi/16$, #2: $\varphi_b = -\pi/2$). (b) The digitized signal and the fitted sinusoidal signal. (c) The errors between the quantized signal and the fitted signal.

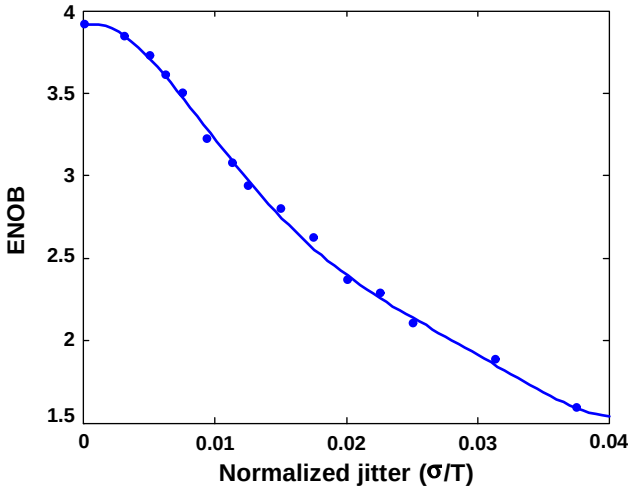


Fig. 5. The ENOB of the system as a function of the standard deviation of the sampling jitter (dots: simulation results; curve: fitted).

laser would lead to the deviation in voltage amplitude, and thus the ENOB degradation. Generally, the amplitude fluctuations δV less than one-half quantization step can be tolerated, as

$$\delta V_{\max} < \frac{V_{\max}}{2^B}, \tag{5}$$

where B is the bit resolution of the system [9]. According to Eq. (5), the allowed maximum fluctuation on the sampling jitter is given by

$$\delta t_{\max} < \frac{1}{2^{B+1}\pi f_{in}}, \tag{6}$$

where a sinusoidal input signal with a frequency f_{in} is assumed. For a 4-bit system with a sinusoidal input signal with a frequency of 4 GHz as in our experiment, the allowed maximum fluctuation in the sampling interval is $\delta t_{\max} = 0.25$ ps.

To clarify the relationship between the sampling jitter and the ENOB degradation, we use the Monte-Carlo method to simulate the process. In the simulation, the overall sampling jitter is considered as a Gaussian distributed random variable, which has the probability density function, *given by*

$$\varphi_\sigma(x) = \frac{1}{\sigma\sqrt{2\pi}}\exp\left(-\frac{x^2}{2\sigma^2}\right), \tag{7}$$

where σ is the standard deviation of the sampling jitter. In the simulation, the sinusoidal input signal is assumed and the sampling jitter σ is normalized to the period T of the input signal. Noise is not considered in our simulation. Simulation results are shown in Fig. 5, where the dots and the curve denote the simulation results and the fitted results, respectively. It is shown that the ENOB degrades with the increase of time jitter. In a system without time jitter, the ENOB is near to the ideal bit resolution, four in this case. When the normalized jitter increases to be 0.04, the ENOB decreases to be around 1.5.

A 4-bit ADC is demonstrated in our experiment. To increase the bit resolution, more MZMs and comparators are required. An ADC with any bit resolution can be obtained if the numbers of MZMs and comparators are properly chosen with the bias phase shifts properly set as discussed previously. Table 1 shows the required numbers of MZMs and comparators for ADCs with different bit resolutions. Compared with the schemes in [2,9], the proposed scheme requires more MZMs when the bit resolution $N_R > 6$. This is the major limitation of the proposed approach. However, an ADC with a bit resolution 4–6 is sufficient for most applications where a sampling rate above 1 GHz is required, such as in advanced radar systems and satellite communications systems [12]. The key advantage of the proposed scheme is that the ADC employs MZMs with identical half-wave voltages (i.e., identical electrode lengths), which simplifies greatly the practical realization compared with the schemes in [2,9].

Table 1
Number of MZMs and comparators required for realizing ADCs with different bit resolution.

Bit resolution	Number of MZMs	Number of comparators
4-bit	2	9
5-bit	3	17
6-bit	5	33
n-bit	$2^{n-4}+1$	$2^{n-1}+1$

As discussed earlier, the schemes in [3,4] also use optical modulators with identical half-wave voltages. Compared with the schemes in [3,4] using cascaded modulators, however, the proposed approach features a simpler system architecture with a parallel design, which eliminates the problems such as nonuniform loss for the channels and the requirement for accurate synchronization between the electrical and the optical signals at the cascading modulators.

4. Conclusions

In this paper, a novel scheme to realize photonic ADC using MZMs with identical V_π and multiple comparators was proposed and demonstrated. Compared with the scheme using MZMs with geometrically scaled V_π, the proposed approach has a major advantage of using MZMs with identical half-wave voltages, which simplify significantly the implementation. The bit resolution was improved by using multiple comparators for each MZM channel without increasing the number of MZMs. The digital coding was realized based on the SNS technique. A proof-of-concept experiment was implemented, where analog-to-digital conversion with a 4-bit resolution using two MZMs and nine comparators was demonstrated. The ENOB degradation induced by the sampling jitter was numerically studied based on the Monte-Carlo simulation.

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