

Photonic analog-to-digital converter using Mach–Zehnder modulators having identical half-wave voltages with improved bit resolution

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A novel approach to perform photonic analog-to-digital conversion with improved bit resolution is proposed and investigated. Instead of using Mach–Zehnder modulators (MZMs) with geometrically-scaled half-wave voltages, the MZMs in the approach have identical half-wave voltages, which greatly simplifies the implementation. To improve the bit resolution without increasing the number of MZMs, each MZM is connected with multiple comparators having multiple thresholds. The quantization and encoding are performed based on the symmetrical number system (SNS) technique. Three new quantization and encoding schemes based on the SNS are proposed and demonstrated. A 4 bit photonic analog-to-digital conversion based on the given schemes is investigated. For the given schemes, two MZMs are needed with the numbers of comparators being 14, 16, and 9, respectively. Numerical simulations and experiments are performed. The effectiveness of the proposed schemes is verified. © 2009 Optical Society of America

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1. Introduction

The implementation of analog-to-digital conversion in the optical domain has been a topic of interest for a few decades, thanks to the numerous advantages over the conventional electronic analog-to-digital conversion techniques, such as high sampling rate, ultranarrow pulse width, and low timing jitter. In addition, in a photonic analog-to-digital converter (ADC), the back-coupling between the optical pulses and the electrical signal being sampled is small and negligible. Photonic ADCs can be potentially applied to broadband wireless communications, high resolution radar, radio astronomy, and other applications

with extreme bandwidth requirements. Numerous schemes for photonic analog-to-digital conversion have been proposed and demonstrated [1–6]. A well-known architecture to implement a photonic ADC was proposed by Taylor [7,8], in which a parallel array of Mach–Zehnder modulators (MZMs) are used with an input signal applied in parallel to the MZMs, which is sampled at the MZMs by an optical pulse train. The MZMs employed differ in electrode lengths by a factor of two for two adjacent channels and, therefore, with geometrically-scaled half-wave voltages. The sampled signal is sent to an array of photodetectors (PDs) and then applied to an array of high-speed binary comparators to produce a digital Gray-code output. In this scheme, an array of n MZMs can provide an n -bit resolution. For practical applications, a bit resolution of eight or higher is

often required. However, a resolution higher than 4 bit is hard to achieve in Taylor's scheme since the electrode length of the MZM corresponding to the least significant bit (LSB) is very long, which is hard to fabricate with the currently available technology. To avoid using MZMs with a long electrode length, a few modified system structures have been proposed [9–12]. Jalali and Xie [9] and Currie [10] proposed using cascaded MZMs and distributed phase modulators. Stigwall and Galt proposed a scheme to use a free-space interferometric structure with a phase modulator in one arm [11]; the same concept was recently demonstrated by Li *et al.* based on a fiber-optic platform [12].

Recently, a new approach that uses an array of MZMs with identical half-wave voltages was proposed and demonstrated in [13]. Since the MZMs employed were with identical half-wave voltages, the system was greatly simplified. A major limitation of the technique in [13] is its low bit resolution. For an ADC with n MZMs, the number of the quantization levels is only $2n$ and, therefore, it has a bit resolution of $N_R = \log_2(2n)$.

On the other hand, an ADC with an improved resolution can be achieved by using multiple threshold levels. In [14], a concept that uses several threshold values to extend the resolution of an optical ADC was proposed. In the scheme, for one MZM channel, a number of comparators with different threshold values were employed to quantize and encode the sampled signal using a technique called symmetrical number system (SNS) [14]. It was shown that by utilizing multiple comparators based on the SNS theory, a bit resolution larger than one for each channel can be obtained. For example, to realize a 4 bit ADC, only two MZMs are required, while in [11–13] eight MZMs or phase modulators are needed. In the scheme, to resolve the ambiguity problem when the SNS technique was used, the MZMs should be designed to have different half-wave voltages.

The approach demonstrated in this paper employs MZMs with identical half-wave voltages and multiple comparators. This concept was first proposed by us in [15]. To increase the bit resolution while maintaining a small number of MZMs, multiple comparators for each MZM are used. The quantization and encoding are performed based on the SNS technique. Instead of using MZMs with different half-wave voltages, we propose to employ MZMs with identical half-wave voltages but which are biased at different bias points. Three new quantization and encoding schemes based on the SNS technique are demonstrated in this paper. A 4 bit ADC based on the given schemes is investigated. To achieve a 4 bit resolution, for all three schemes, only two MZMs are needed. The numbers of comparators for the given schemes are 16, 14, and 9, respectively. Numerical simulations and proof-of-concept experiments are performed. The feasibility and effectiveness of the proposed schemes are verified.

The remainder of the paper is organized as follows. In Section 2, a brief introduction to photonic ADC using MZMs with identical half-wave voltages is provided. The use of multiple comparators based on the SNS technique for improving the bit resolution is detailed. In Section 3, three different quantization and encoding schemes based on the SNS technique are given. In Section 4, the given three schemes are investigated by numerical simulations and proof-of-concept experiments. Discussions on the conversion of the code bits, the code properties, the influence of the sampling timing jitter, and the noise on the system performance are provided in Section 5. A conclusion is drawn in Section 6.

2. Principle

We have recently proposed and experimentally demonstrated a photonic ADC using an array of MZMs with identical half-wave voltages, which reduces significantly the complexity of the system and makes the practical realization possible [13].

Figure 1 shows the schematic of a photonic ADC with four MZMs having identical half-wave voltages [13]. Each MZM is connected by one comparator with a threshold set at half of the full scale. The MZMs are biased such that the transfer functions of the MZMs are uniformly shifted, which leads to the generation of a linear binary code to represent the sampled analog signal. The operation principle is shown in Fig. 2. For an ADC with four channels, the four MZMs are biased with their transfer functions shifted laterally with a uniform phase spacing of $\pi/4$. The outputs from the comparators with a threshold level at half of the full scale are shown in Fig. 2(b). The quantized values of the signal at the output of the 4-channel ADC are shown in Fig. 2(c).

This architecture makes use of the dependence of the output optical intensity on the bias voltage applied to the MZMs and the voltage of the RF signal. The advantage of the approach is that all the MZMs employed have identical electrode lengths, eliminating the requirements for the doubling of the electrode length for an MZM of the next significant bit (NSB), thereby greatly simplifying the implementation.

In the approach, the normalized optical intensity at the output of an MZM with a half-wave voltage

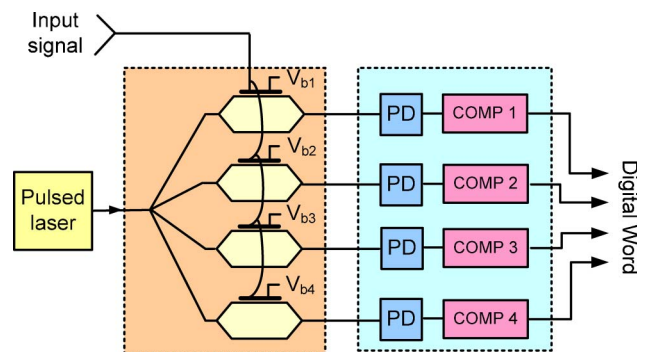


Fig. 1. (Color online) 3 bit ADC using four MZMs with identical half-wave voltages.

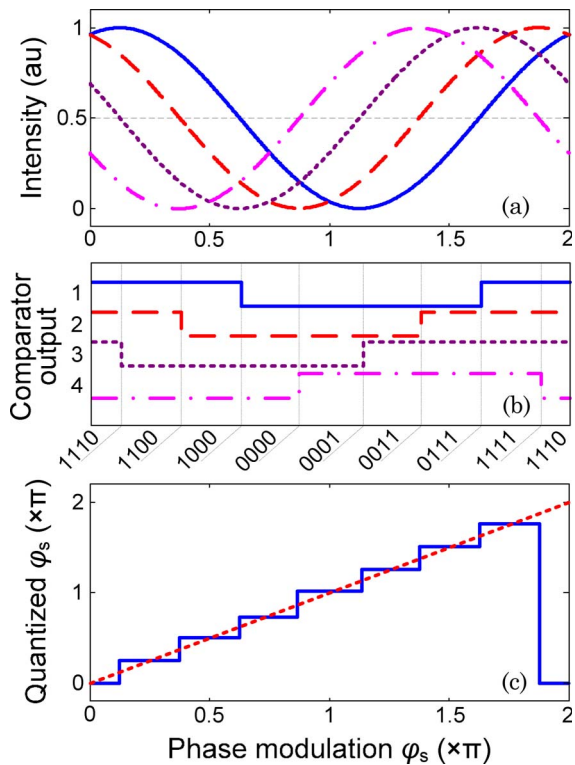


Fig. 2. (Color online) Operation of a 4-channel photonic ADC. (a) Transfer functions of the four MZMs: dash-dot, $\varphi_b = 0$; dotted, $\varphi_b = \pi/4$; dash, $\varphi_b = 2\pi/4$; solid, $\varphi_b = 3\pi/4$. (b) Quantization operation. (c) Relationship between the input phase modulation (dotted) and the quantized values (solid).

V_π can be determined by both the voltage of the analog signal to be digitized and the applied bias voltage,

$$I_0 = \frac{I_i}{2} [1 + \cos(\varphi_s + \varphi_b)], \quad (1)$$

where I_i is the input optical intensity, $\varphi_s = \pi V_s(t)/V_\pi$ is the phase shift introduced by the RF signal $V_s(t)$, and $\varphi_b = \pi V_b/V_\pi$ is the phase shift introduced by the bias voltage V_b .

To get a uniform quantization, the bias voltages applied to the MZMs should be set to have uniform phase spacing. Their values depend on the number of the MZMs employed.

For an ADC with four channels, the code length is only 8, or a resolution of 3 bit. To achieve a bit resolution of four, the number of MZMs has to be increased to eight, which significantly increases the complexity and cost of the system. To increase the bit resolution while employing MZMs with identical half-wave voltages, we propose to use multiple comparators at the output of each MZM with each comparator set at a different threshold level [15]. Figure 3 shows a schematic of the proposed ADC with n channels. As can be seen, the ADC is identical to that shown in Fig. 1 except that the output of each MZM is sent to k comparators. The use of multiple comparators has been proposed by Pace and Styer to improve the bit resolution [14]. In [14], the digitization is performed

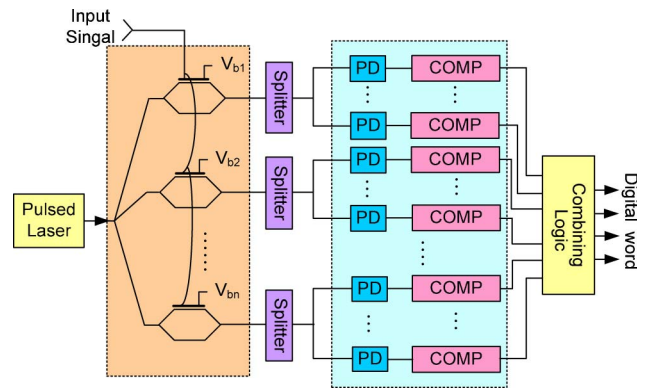


Fig. 3. (Color online) n -channel ADC with n MZMs having identical half-wave voltages. The resolution is improved by using multiple comparators at the output of each MZM.

based on the SNS theory. To resolve the ambiguity problem in the encoding process, the MZMs should be designed to have slightly different electrode lengths (which means different half-wave voltages), which complicates the practical implementation. The key difference between our approach and the approach proposed by Pace and Styer is that we use MZMs with identical half-wave voltages, and the ambiguity problem is resolved by properly biasing the MZMs.

As can be seen, the sampled signal from each MZM is connected to a splitter that divides the sampled signal into k copies. Each copy is converted to an electrical signal at a PD and then digitized by a comparator with a specific threshold for the MZM. Then, the outputs from the comparators are sent to a combining logic module to change the $n \times k$ code bits into the needed binary code. The encoding process is described in detail in Section 3.

3. Encoding Schemes Based on the SNS

As proposed by Pace and Styer, the outputs from the multiple comparators can be encoded based on the SNS [14]. Here we propose three different SNS encoding schemes that are designed to fit the architecture using MZMs with identical half-wave voltages.

A. Scheme I

In the SNS encoding scheme proposed by Pace and Styer [14], a positive integer modulus m is used to denote the intensity of the sampled signal. For a given m , the integer values within twice the individual modulus ($2m$) are given by $[0, 1, 2, \dots, m-1, m-1, \dots, 2, 1, 0]$, from which we can see that the SNS folding waveform is symmetric about the midpoint. Because of the symmetric nature, two intensities may be represented by one integer, leading to an ambiguity. In [14], the encoding ambiguity problem was solved by using MZMs with slightly different electrode lengths or half-wave voltages.

For an n -channel ADC, if the SNS scheme is used to quantize and encode the sampled signal, for a given m , $m-1$ comparators are needed for each MZM. An n -channel ADC with n MZMs will have $n \times (m-1)$ comparators. To avoid the encoding

ambiguity problem, we propose to bias the MZMs with a phase shift. If the bias phase shift applied to each MZM is

$$\varphi_b^j = -\frac{j2\pi}{mn}, \quad (j = 0, 1, 2, \dots, n-1). \quad (2)$$

The number of quantization level is $M = mn$, and the bit resolution is given by $N_R = \log_2(mn)$.

For the output optical intensity from an MZM given by Eq. (1), the normalized threshold values are

$$T_j = \cos^2 \left[\frac{\pi}{2mV_j} + \frac{\pi}{2} \right], \quad (3)$$

where $V_j \in \{1, 1/2, 1/3, 1/4, \dots, 1/(m-1)\}$.

For each comparator, the output is “1” if the input signal is greater than the preset threshold, and the output is “0” if the input signal is smaller. The digital word can be obtained by comparing the signal intensity with the preset thresholds.

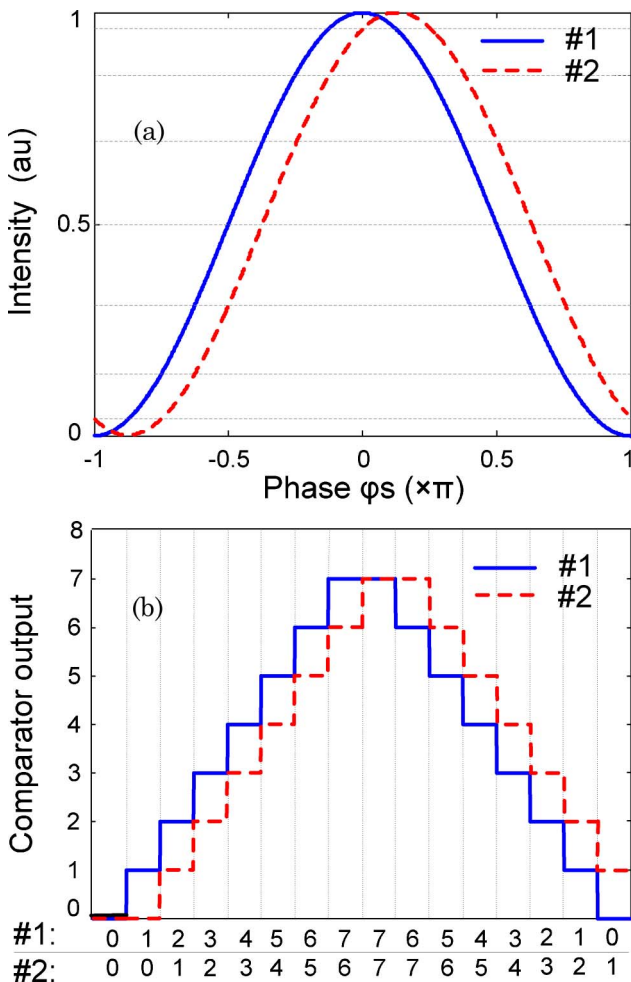


Fig. 4. (Color online) (a) Transfer functions of the two MZMs: solid line, $\varphi_b = 0$; dash line, $\varphi_b = -\pi/8$. (b) Quantization operation using the proposed Scheme.

Take a 2-channel ADC with an integer modulus $m = 8$ as an example, two MZMs and 14 comparators are required. The transfer functions of the two MZMs are shown in Fig. 4(a), in which the horizontal axis is the phase shift induced by the input RF signal and the vertical axis denotes the normalized intensity of the output optical signal. The horizontal dashed lines indicate the seven threshold values for the two channels. The threshold values are varied depending on the number of the comparators according to Eq. (3). By comparing the values between the intensity of the signals and the preset threshold values, we obtain the SNS comparator output (thermometer code), which is cyclic in nature, as shown in Fig. 4(b).

As discussed above, the resolution of the ADC depends on the numbers of the MZMs and the comparators. Generally, for the case of $m = 8$, to achieve a resolution of n bit, 2^{n-3} MZMs and $2^{n-3} \times 7$ comparators are needed. Clearly the number of the MZMs and the comparators will be doubled when one more bit is required for a given number of threshold values. To reduce the complexity of the system, an improved scheme is proposed in Subsection 3.B.

B. Scheme II

Similar to the encoding scheme in Section 3.A, Scheme II also uses an integer modulus m to indicate the intensity of the sampled signal, and the integers within each modulus also represent a symmetrically folded waveform. The major difference is that an additional integer m is added to each individual modulus. For a given m , the integer values within twice the individual modulus ($2m$) are given by $[0, 1, 2, \dots, m-1, m, m-1, \dots, 2, 1]$.

For a given integer modulus m , m comparators are needed for each MZM. With the output signal given by Eq. (1), the preset threshold values for the comparators are given by

$$T_j = \cos^2 \left[\frac{\pi}{2mV_j} + \frac{\pi}{2} - \frac{\pi}{4m} \right], \quad (4)$$

where $V_j \in \{1, 1/2, 1/3, 1/4, \dots, 1/m\}$. If the input signal is greater than the preset threshold, the output is “1,” otherwise the output is “0.” The number of output “1” in all channels can be used to uniquely denote the input signal intensity.

The bias phase shift applied to each MZM should be

$$\varphi_b^j = -\frac{j\pi}{m(n-1)} - \frac{\pi}{16}, \quad (j = 0, 1, 2, \dots, n-1). \quad (5)$$

The number of quantization levels is $M = 2m(n-1)$, and the bit resolution is given by $N_R = \log_2[2m(n-1)]$.

Again, take a 2-channel ADC with an integer modulus $m = 8$ as an example. The transfer functions of the two MZMs are shown in Fig. 5(a). The dashed lines indicate the needed eight threshold values. Comparing the signal intensity and the preset

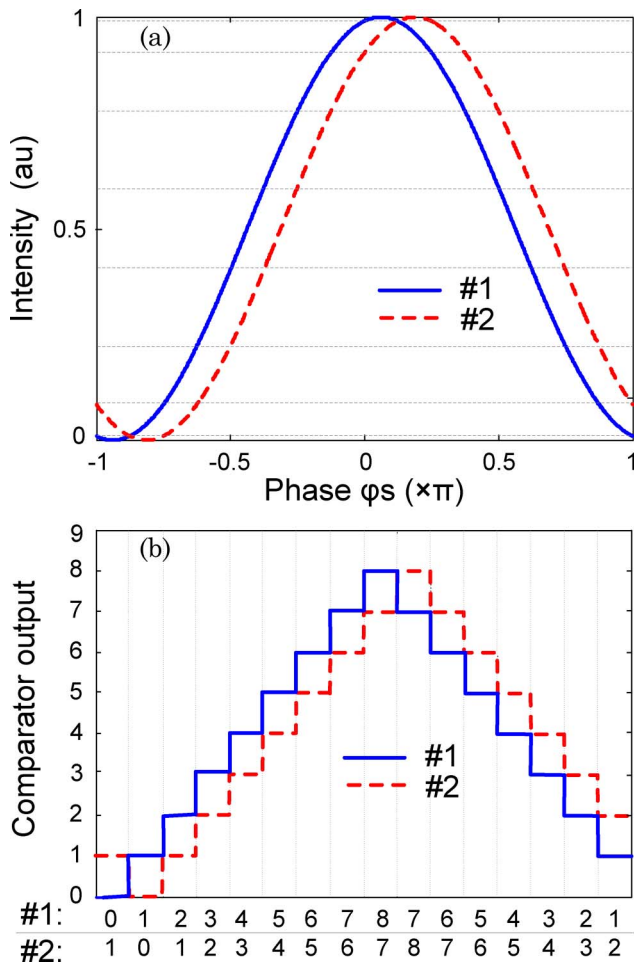


Fig. 5. (Color online) (a) Transfer functions of the two MZMs: solid line, $\varphi_b = -\pi/16$; dashed line, $\varphi_b = -3\pi/16$. (b) Quantization operation using Scheme II.

threshold values, the phase that is changed with the signal intensity can be divided into 16 quantization levels, which are expressed in the form of the digital words as [01 10 21 32 43 54 65 76 87 78 67 56 45 34 23 12], as shown in Fig. 5(b).

In Scheme I, for a given number of the threshold levels, the numbers of the MZMs and comparators have to be doubled if one more bit is to be added. For example, if the number of the threshold levels is seven, two more channels are needed to meet the demand for another 16 quantization levels. For the case of Scheme II, for a given modulus m , the integer values within twice the individual modulus ($2m$) are asymmetric. For a given number of the threshold levels, to increase the quantization levels from $2m$ to $4m$, only one more channel is needed to uniquely denote the intensity of the input signal. That is, m more comparators and one more MZM should be added. Therefore, to achieve a higher resolution, an ADC implemented based on Scheme II has a simpler configuration than an ADC based on Scheme I. Generally, in Scheme II, $2^{n-4} + 1$ MZMs and $2^{n-1} + 8$ comparators are required to achieve a resolution of n bit for the case of $m = 8$.

C. Scheme III

To further simplify the structure of a photonic ADC, a third scheme is proposed. In an ADC based on Scheme III, one of the MZM channels with multiple comparators is replaced by a channel with only one comparator, the threshold of which is set as the half of the full scale. Note that this one-threshold channel should have a bias phase shift $\varphi_b = -\pi/2$, while the bias phase shift of other channels is still set according to Eq. (5). The digital word obtained based on this scheme can still uniquely denote the intensity of the input signal, while keeping the original bit resolution. The total number of the comparators required in an ADC based on Scheme III is reduced by $m - 1$.

To demonstrate the concept more clearly, a simple example of a 4 bit ADC with $n = 2$ and $m = 8$ is provided. The first channel has eight comparators with the threshold values determined by Eq. (4), and the second channel has one comparator with a threshold set at half of the full scale. The bias phase shifts of the two channels are $-\pi/16$ and $-\pi/2$. Figure 6(a) shows the transfer functions of the two MZMs. The eight thresholds for channel 1 are denoted by the

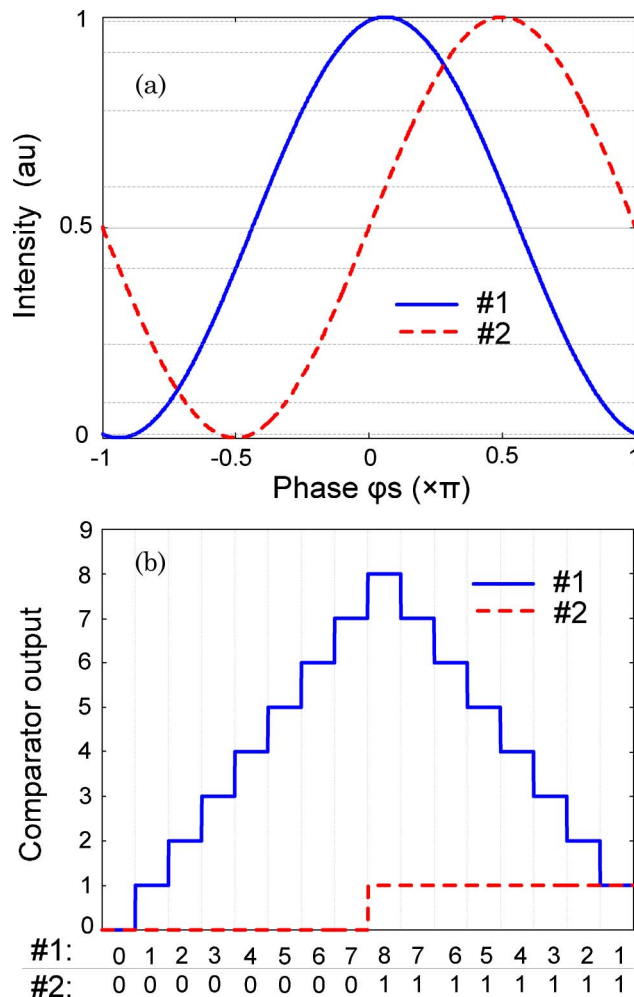


Fig. 6. (Color online) (a) Transfer functions of the two MZMs: solid line, $\varphi_b = -\pi/16$; dash line, $\varphi_b = -\pi/2$. (b) Quantization operation using Scheme III.

horizontal dashed lines and the one threshold for channel 2 is denoted by the horizontal solid line in Fig. 6(a). For each phase shift value induced by the input RF signal, the number of output “1” for each channel can be calculated by comparing the signal intensity with the preset thresholds. The digital codes can be obtained from the numbers of output “1,” as shown as the solid curve [0 1 2 3 4 5 6 7 8 7 6 5 4 3 2 1] and the dash curve [0 0 0 0 0 0 0 0 1 1 1 1 1 1 1] for the phase from $-\pi$ to π . Therefore, from Fig. 6(b) we can see that the representation of the phase from $-\pi$ to π in digital words is given by [00 10 20 30 40 50 60 70 81 71 61 51 41 31 21 11], in which the combination of two digital words corresponds to the 16 quantization levels. A bit resolution of four is thus achieved.

If we choose the proper numbers of the MZMs and the comparators, with the MZM being properly biased to have the required bias phase shifts, an ADC with arbitrary bit resolution can be achieved. Generally, $2^{n-4} + 1$ MZMs and $2^{n-1} + 1$ comparators are needed in Scheme III to realize a resolution of n bit. A comparison of the required numbers of MZMs and comparators among the three schemes, for the case of $m = 8$, is given in Table 1.

4. Results

Here we investigate a 4 bit photonic ADC with the quantization and encoding implemented based on the three schemes proposed in Section 3. Numerical simulations and experimental verifications are performed. Figure 7 shows the experimental setup. The light wave generated by a tunable laser source (Yokogawa AQ2201) operating at 1550 nm is sent to a 20 GHz JDS-Uniphase intensity modulator through a polarization controller (PC). The PC is adjusted to minimize the polarization-dependent loss in the modulator. A 45 GHz PD is used to implement the optical/electrical conversion. To prove the concept, the modulator is driven by a 4 GHz sinusoidal signal generated by a signal generator (Agilent E8254A). A digital sampling oscilloscope (Agilent 86116A) is used to capture the temporal waveforms, which is triggered by the signal generator. The half-wave voltage V_π of the modulator is 9.2 V.

In the experiment, we emulate the output characteristics of a 2-channel ADC by tuning the bias voltage of the modulator with a constant step $V_\pi/8 =$

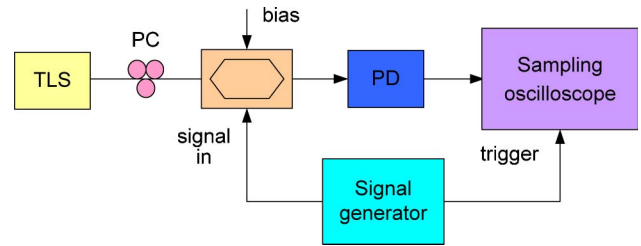


Fig. 7. (Color online) Experimental setup: TLS, tunable laser source; PC, polarization controller; PD, photodetector.

1.2 V. In the three examples, the channel number n is 2, the bit resolution N_R is 4. For each bias voltage, we measure and record the waveform by the oscilloscope. Based on the recorded waveforms, we use a program to sample the waveforms to get discrete intensity data at a fixed time interval. Then, a digitized signal is obtained by comparing the sampled data with the threshold values. It should be noted that the problems of synchronization and timing jitter do not exist due to the use of the software sampling. In practical realization, all optical channels should be finely tuned to achieve a precise synchronization. The jitter-induced degradation is discussed in Section 5.C.

A. Scheme I

We first investigate a 4 bit photonic ADC with an architecture based on Scheme I, where n is equal to 2 and k is equal to 7. To implement the ADC, two MZMs, two splitter, 14 PDs, and 14 comparators have to be used. The bias voltages applied to the MZMs are set to ensure a phase spacing of $\Delta\varphi_b = \pi/8$ according to Eq. (2); the corresponding transfer functions of the two MZMs are shown in Fig. 4(a).

For each channel, seven comparators are used. The normalized threshold values according to Eq. (3) are given by

$$T_j = \cos^2 \left[\frac{\pi}{2 \times 8V_j} + \frac{\pi}{2} \right], \quad (6)$$

where $V_j \in \{1, 1/2, 1/3, 1/4, 1/5, 1/6, 1/7\}$.

Using the transfer functions shown in Fig. 4(a), we obtain the comparator outputs. The input voltage is quantized into 16 quantization levels with each level represented by a different number. Therefore, different digital words result.

Figure 8 shows the numerical results of the 4 bit ADC based on Scheme I. Figure 8(a) shows the signals at the outputs of the MZMs, with the MZMs biased to have $\varphi_b = 0$ and $\varphi_b = -\pi/8$. Comparing the intensity of the signals with the threshold values given by Eq. (6), the signal is quantized, which is shown by the stepped line in Fig. 8(b). The errors between the quantized and the input signals are given in Fig. 8(c).

The simulation results are then verified by an experiment. By adjusting the bias voltages to make $\varphi_b = 0$ and $\varphi_b = -\pi/8$, we recorded two traces (without averaging) of the output signals, which

Table 1. Comparison of the Required Number of MZMs and Comparators Among the Three Schemes^a

Resolution (bits)	Number of MZMs			Number of Comparators		
	I	II	III	I	II	III
4	2	2	2	14	16	9
5	4	3	3	28	24	17
6	8	5	5	56	40	33
n	2^{n-3}	$2^{n-4} + 1$	$2^{n-4} + 1$	$2^{n-3} + 1$	$2^{n-1} + 1$	$2^{n-1} + 1$

^a $m = 8$

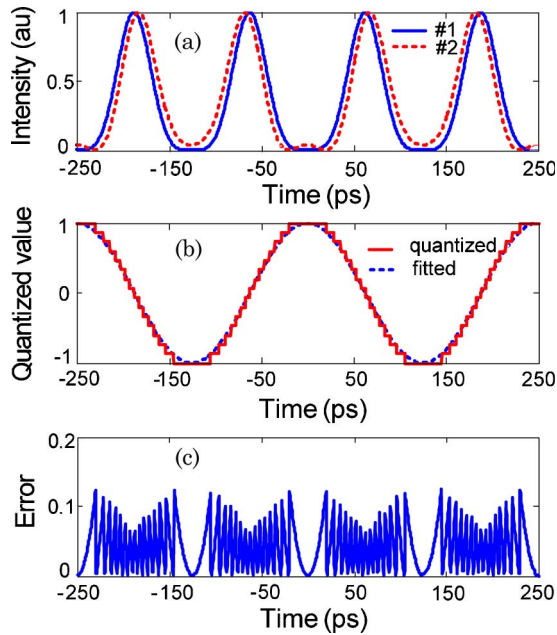


Fig. 8. (Color online) Numerical result for an ADC based on Scheme I. (a) Two ideal output waveforms corresponding to two bias phase shifts: solid line, $\varphi_b = 0$; dash line, $\varphi_b = -\pi/8$. (b) Quantized signal (stepped) and the fitted sinusoidal signal (smooth). (c) Errors between the quantized signal and the fitted signal.

are shown in Fig. 9(a). The quantized signal is shown in Fig. 9(b). As a comparison, a fitted sinusoidal signal is also shown in Fig. 9(b). Note that the maximum quantized value is 1, which is equivalent to a phase shift of $1.625\text{--}1.75\pi$. The maximum phase shift is determined by the maximum power of the input RF signal. Figure 9(c) shows the errors between the quantized signal and the fitted signal. Because of the noise in the detected waveforms, errors in some sampling points are larger than the magnitude of the LSB.

Based on the errors between the quantized values and the fitted signal, the digital signal-to-noise ratio (dSNR) is estimated to be around 214 (23.3 dB), which corresponds to an effective number of bits (ENOB) of 3.6, according to the following formula [6]:

$$\text{ENOB} = \frac{\text{dSNR} - 1.76}{6.02}. \quad (7)$$

Since the bit resolution of the system is 4, the ENOB deviation from the ideal case is 0.4. This ENOB degradation is owing to the noise sources in the system, which includes the relative intensity noise (RIN) of the laser source, the shot noise and the thermal noise of the PD, and the instrument noise.

B. Scheme II

Then, we investigate a 4 bit photonic ADC with an architecture based on Scheme II, where n is 2 and k is 8. The only difference between the ADCs based on Scheme I and Scheme II is that the ADC based on Scheme II requires the use of 16 comparators.

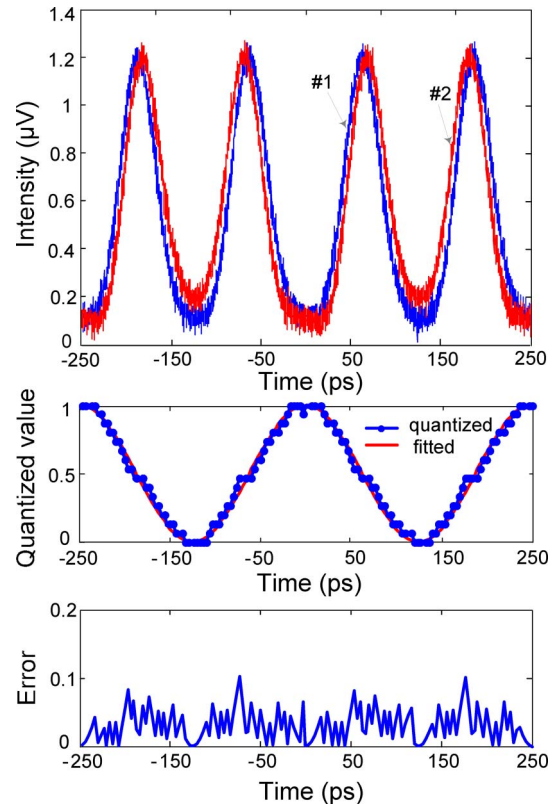


Fig. 9. (Color online) Experimental results for a 4 bit ADC based on Scheme I. (a) Measured two waveforms corresponding to two bias phase shifts ($\varphi_b = 0$ and $\varphi_b = -\pi/8$). (b) Quantized signal (stepped) and the fitted sinusoidal signal (smooth). (c) Errors between the quantized signal and the fitted signal.

Similar to the ADC based on Scheme I, the uniform phase spacing between the bias voltages applied to the MZMs is set with $\Delta\varphi_b = \pi/8$; the transfer functions of the two MZMs are shown in Fig. 5(a). The normalized threshold values according to Eq. (4) are

$$T_j = \cos^2 \left[\frac{\pi}{2 \times 8 V_j} + \frac{\pi}{2} - \frac{\pi}{4 \times 8} \right], \quad (8)$$

where $V_j \in \{1, 1/2, 1/3, 1/4, 1/5, 1/6, 1/7, 1/8\}$.

The comparator outputs are obtained by comparing the signal intensity and the thresholds.

Since the uniform phase spacing between the bias voltages applied to the MZMs is also set with $\Delta\varphi_b = \pi/8$ (the same as Scheme I), the ADC would have the same quantization errors, as shown in Fig. 8.

An experiment is then performed. The experimental setup is the same as the one shown in Fig. 7, and the experimental data used in Example I are also applied here, as shown in Fig. 9(a). Figures 10(a) and 10(b) shows the experimental results and the errors between the quantized values and the fitted signal.

According to Eq. (7), the dSNR is estimated to be around 171 (22.3 dB), which corresponds to an ENOB of 3.4, but the bit resolution N_R of the system is 4, the

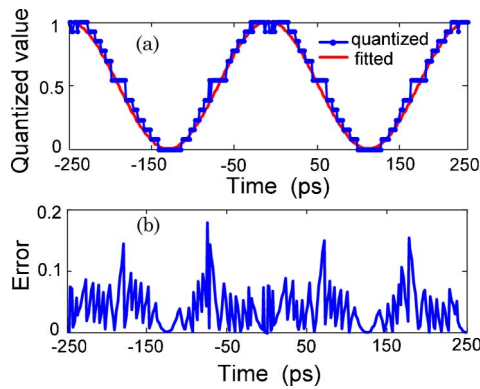


Fig. 10. (Color online) Experimental results for a 4 bit ADC based on Scheme II. (a) Digital signal (stepped) and the fitted sinusoidal signal (smooth). (b) Errors between the quantized signal and the fitted signal.

ENOB deviation from the ideal case is 0.6. Again, this deviation is due to noise sources in the system.

Compared with Scheme I, an ADC-based Scheme II provides the same performance in terms of quantization errors. However, as discussed earlier, for an ADC with a resolution higher than 4, to achieve the same bit resolution an ADC based on Scheme II has a simpler architecture.

C. Scheme III

Finally, we investigate a 4 bit ADC with an architecture based on Scheme III. As discussed in Subsection 3.C, a 4 bit ADC based on Scheme III requires using two MZMs and nine comparators, with one MZM connected by a single comparator with its threshold set at half of the full scale.

Using the quantization and encoding method according to Scheme III, the bias voltages applied to the MZMs should be adjusted to make a phase difference between the two MZMs of $7\pi/16$. The corresponding transfer functions of the two MZMs are shown in Fig. 6(a). The quantization threshold values of one channel with eight comparators are set according to Eq. (6), the quantization threshold for the other channel is set as half of the full scale. The simulation results are shown in Fig. 11.

Then, the simulation results are verified by an experiment. The MZMs are biased such that the phase shift between the two channels is $7\pi/16$. Two recorded waveforms corresponding to two bias phase shifts are shown in Fig. 12(a). The quantization and encoding are performed based Scheme III. The digitized signal and the fitted waveform are shown in Fig. 12(b). Figure 12(c) gives the errors between the quantized signal and the fitted signal.

Based on the errors between the quantized values and the fitted signal, the dSNR is estimated to be around 211 (23.2 dB), which corresponds to an ENOB of 3.6. The deviation from the ideal case is thus 0.4.

5. Discussions

In Section 4, a photonic ADC implemented based on the three proposed quantization and encoding

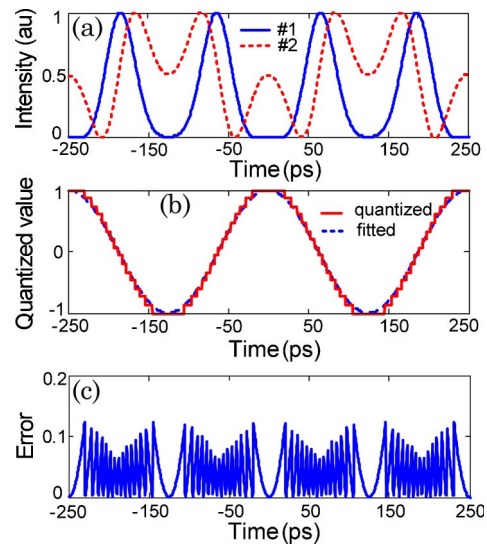


Fig. 11. (Color online) Numerical results for a 4 bit ADC based on Scheme III. (a) Two ideal output waveforms corresponding to two bias phase shifts: solid, $\varphi_b = -\pi/16$; dash, $\varphi_b = -\pi/2$. (b) Quantized signal (stepped) and the fitted sinusoidal signal (smooth). (c) Errors between the quantized signal and the fitted signal.

schemes were investigated. Since the quantization and encoding are based the SNS technique, the output digital words are encoded as a thermometer code. Therefore, a conversion from a thermometer code to a binary code is needed.

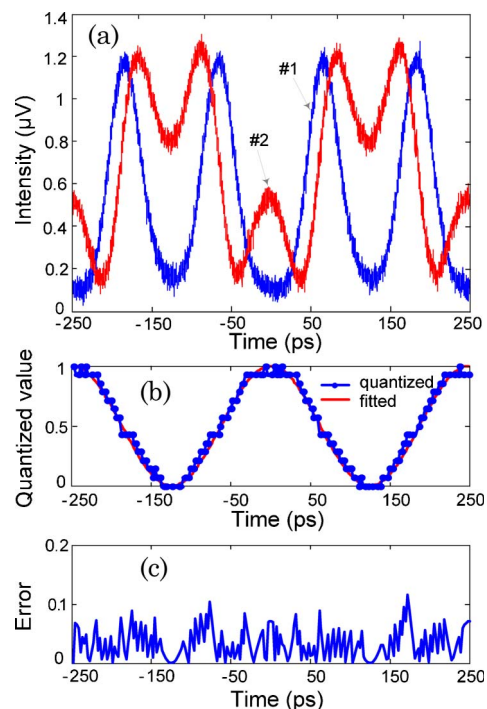


Fig. 12. (Color online) Experimental results for a 4 bit ADC based on Scheme III. (a) Measured two waveforms corresponding to two bias phase shifts of $\varphi_b = -\pi/16$ and $\varphi_b = -\pi/2$. (b) Digital signal (stepped) and the fitted sinusoidal signal (smooth). (c) Errors between the quantized signal and the fitted signal.

A. Code Properties

Different from the commonly used binary codes, the codes generated by the proposed ADC have much more bits. It is composed of “0” and “1,” and the number of “1”s denotes the input signal intensity. The code is usually called a thermometer code [14]. In contrast to the Gray code, the thermometer code changes in two code-bit positions at each increment. This increases the possible readout error in the ambiguity region between two digital values.

For example, in an ADC based on Scheme I with two MZMs and 14 comparators, the number of valid code words is 16 in the 2^{14} possible code words. There are $2^{14} - 16$ invalid code words, and consequently, there is a set of invalid words that has to be handled in case of an erroneous readout.

When processing the experimental data, the occurrence of the invalid words has a high frequency. In our case, we process invalid words in a manner similar to the method given in [16]. Take Scheme III as an example, the invalid words can be divided into three categories. In the first case, the invalid word just has 1 bit that is different from the valid word. We can set the value as the nearest valid word. For instance, we can set an invalid word [1 0 0 0 0 0 0 0] as a valid word [0 0 0 0 0 0 0 0]. In the second case, the invalid word has 1 bit that is different from two valid words. In this case we can set a value at a level that is between the two valid words. For the other cases, which happens at a low probability in practice, there is no way to correct with any accuracy and the best guess would be the valid word at the last sampling point.

Conversion from a thermometer code to a binary code can be achieved using the Karnaugh map [17]. By using a combinational logic circuit, a thermometer code can be directly converted to a binary code.

B. Noise-Induced Degradation

The noise sources in the photonic ADC system include the relative intensity noise from the pulsed laser and the thermal noise and the shot noise from the photodetector. It can be seen from the experimental results that the noises in the obtained waveforms lead to encoding errors and, therefore, a lower ENOB.

To clarify the relationship between the system noise and the ENOB degradation, we perform a computer simulation using the Monte Carlo method to demonstrate the performance of Scheme III under different noise levels. In the simulation, the overall noise in the system is modeled by a Gaussian-distributed random variable, which has the probability density function,

$$\varphi_{\sigma}(x) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left(-\frac{x^2}{2\sigma^2}\right), \quad (9)$$

where σ is the standard deviation of the noise. The modulation depth in the simulation is set to be 1.72π , the same value as in our experimental. For a 4 bit

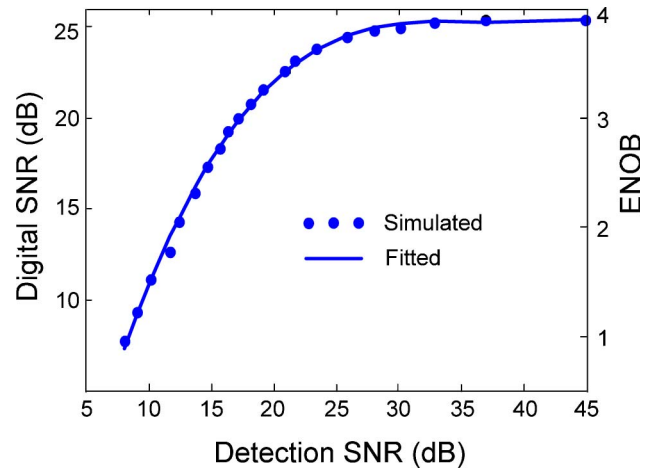


Fig. 13. (Color online) SNR of the digitized signal and the ENOB versus the SNR of the PD current.

ADC based on Scheme III, the simulation result is shown in Fig. 13, where the detection SNR denotes the SNR of the detected waveform of channel 1 (which is related to σ), and the ENOB is related to the dSNR as in Eq. (7). The detection SNR of the obtained waveform (channel 1) shown in Fig. 12(a) is measured to be 22.9 dB. From Fig. 13, we can see that this value corresponds to a dSNR of around 23.7 dB and an ENOB of 3.65, which match well with the measured dSNR of 23.3 dB and ENOB of 3.6.

C. Sampling-Jitter-Induced Degradation

In our experiments, the sampling process is emulated by a software in which ideal sampling, i.e., no sampling jitter, is considered. Note that the deviation in the sampling time originated from the pulsing temporal jitter in a mode-locked laser would lead to a deviation in voltage amplitude and, thus, ENOB degradation.

To show the sampling-jitter-induced ENOB degradation, the encoding process of Scheme III under different levels of timing jitter is simulated using the

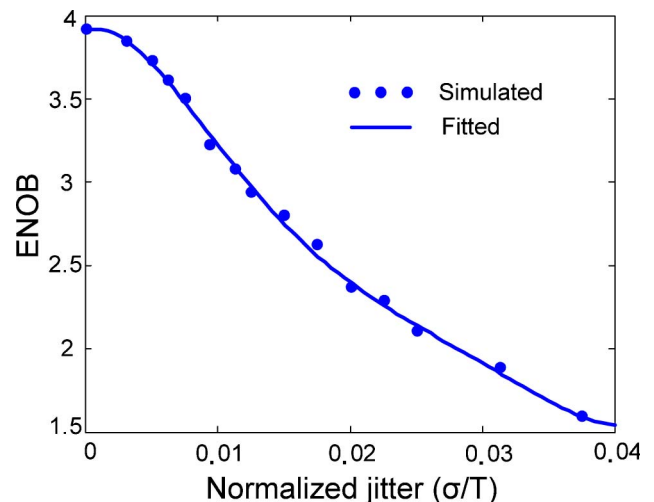


Fig. 14. (Color online) ENOB of the system as a function of the standard deviation of the sampling jitter.

Monte Carlo method. In the simulation, the sampling jitter is considered as a Gaussian-distributed random variable, which has a probability density function given by Eq. (9), in which σ denotes the standard deviation of the sampling jitter. In the simulation, the input signal is assumed sinusoidal and the sampling jitter is normalized to the period T of the input signal. No noise is considered in our simulation. Simulation results are shown in Fig. 14, where the dots and the solid curve denote the simulation results and the fitted results, respectively. It is shown that the ENOB degrades with an increase of timing jitter. In a system without timing jitter, the ENOB is close to the ideal bit resolution, which is 4 in this case. When the normalized timing jitter increases to 0.04, the ENOB decreases to around 1.5.

6. Conclusion

In this paper, a photonic analog-to-digital conversion approach using MZMs with identical half-wave voltages and multiple comparators was presented and discussed in detail. The use of MZMs with identical half-wave voltages makes the practical realization feasible, and the use of multiple comparators effectively improves the bit resolution. Three quantization and coding schemes were presented. The operation principle based on the SNS was presented, which was verified by numerical simulations. In addition, we demonstrated an ADC based on the given coding schemes with 16 quantization levels in proof-of-concept experiments. Experimental results showed that three ENOBs of 3.6, 3.4 and 3.6 for the three schemes, were realized. We further presented the relationship between the system noise and the ENOB degradation based on the Monte Carlo simulation. In addition, the impact of timing jitter of the sampling pulses on the resulting ENOB was also numerically studied.

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