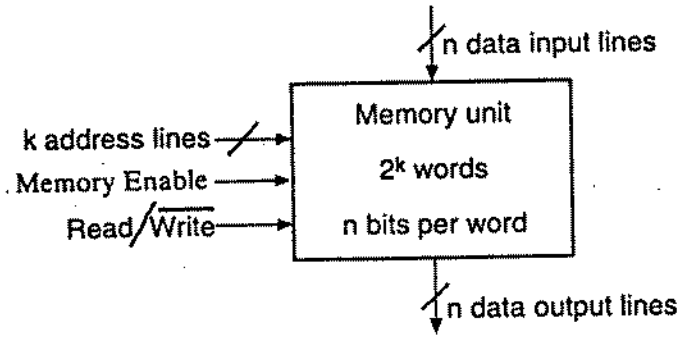
MEMORY UNIT

Memory is a collection of binary storage cells together with associated circuits needed to transfer information into and out of the cells. Memory cells can be accessed to transfer information to or from any desired location, with the access taking the same time regardless of the location, hence, the name *random-access*

A memory unit stores binary information in groups of bits called *words*.



Block Diagram of Memory

Memory address Binary	Memory address Decimal	Memory contents
0000000000	0	10110101 01011100
0000000001	1	10101011 10001001
0000000010	2	00001101 01000110
	⋮	⋮
1111111101	1021	10011101 00010101
1111111110	1022	00001101 00011110
1111111111	1023	11011110 00100100

Contents of a $\underbrace{1024 \times 16}_{2KB}$ Memory

Control Inputs to Memory

Memory Enable	Read/$\overline{\text{Write}}$	Memory Operation
0	X	None
1	0	Write to selected word
1	1	Read from selected word

The steps that must be taken for a write are as follows:

1. Apply the binary address of the desired word to the address lines.
2. Apply the data bits that must be stored in memory to the data input lines.
3. Activate the $\overline{\text{Write}}$ input. ($R/\overline{W}$ = false)

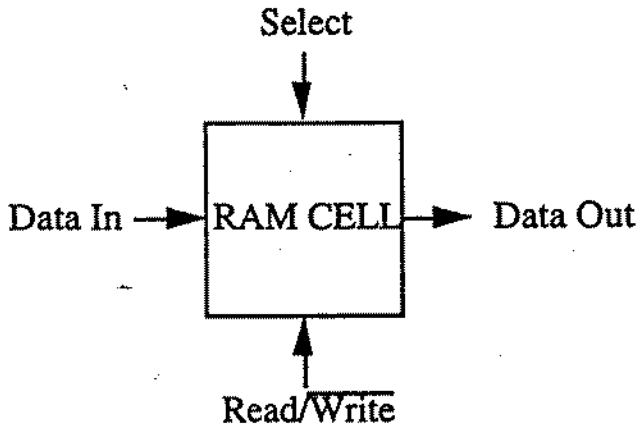
The memory unit will then take the bits from the data input lines and store them in the word specified by the address lines.

The steps that must be taken for a read are as follows:

1. Apply the binary address of the desired word to the address lines.
2. Activate the Read input. ($R/\overline{W}$ = true)

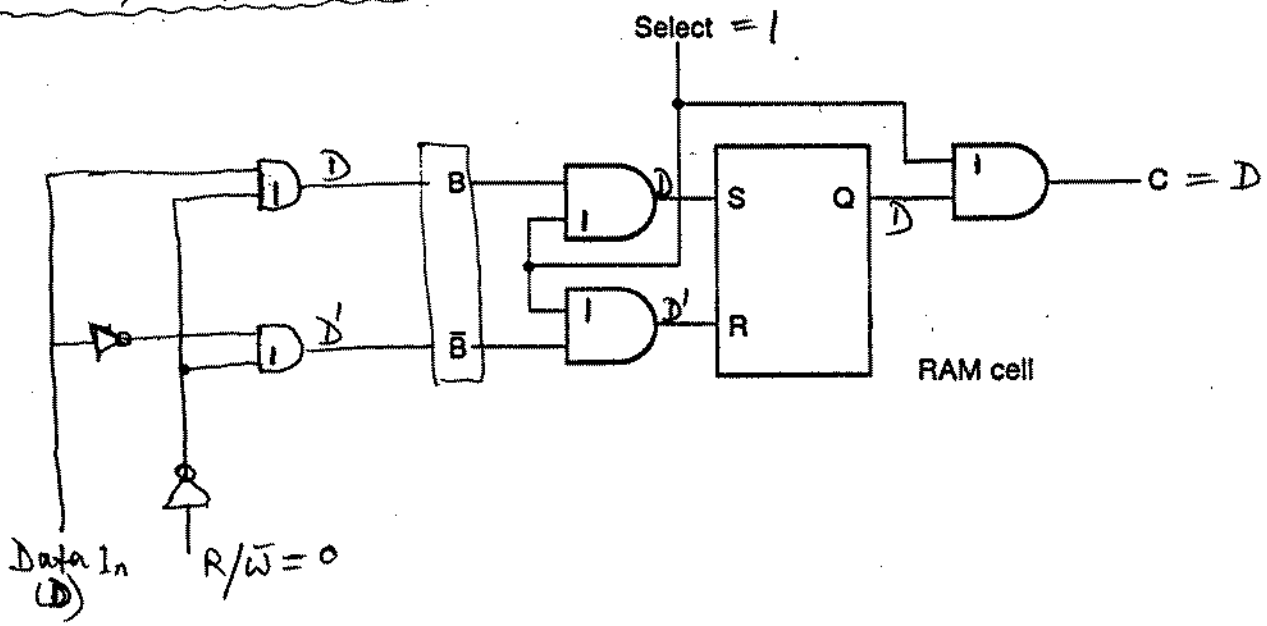
The memory will then take the bits from the word that has been selected by the address and apply them to the data output lines. The contents of the selected word are not changed by reading them.

STRUCTURE OF A RAM CELL

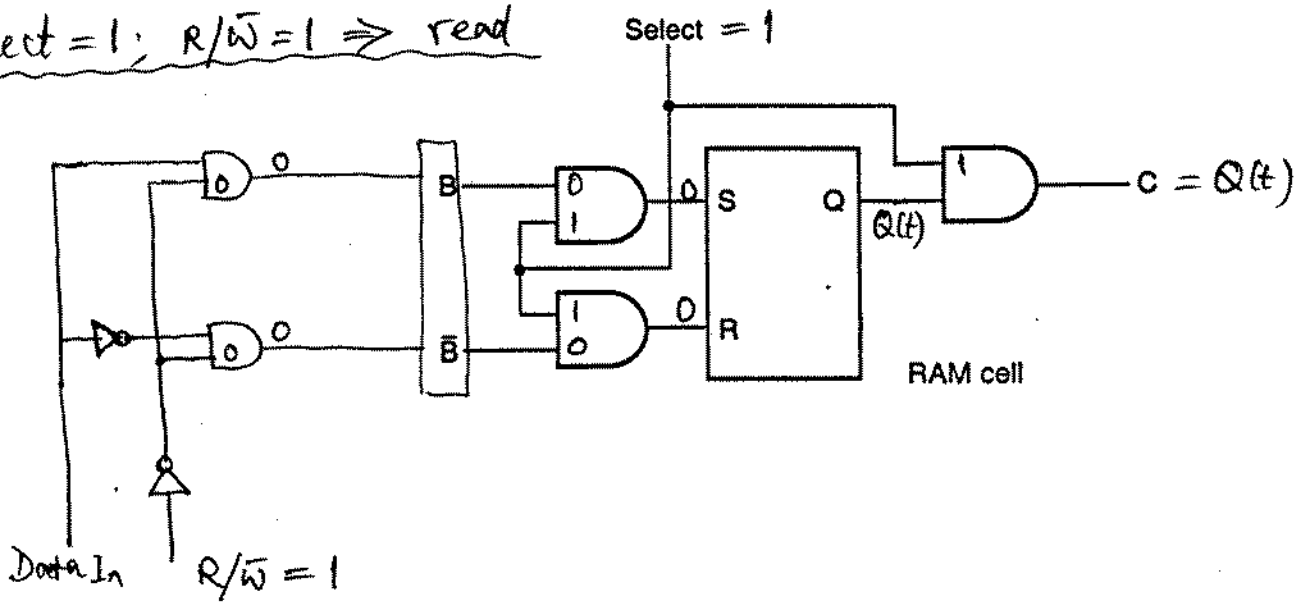


Select = 0 ⇒ No read/write.

Select = 1; R/$\bar{W}$ = 0 ⇒ write



Select = 1; R/$\bar{W}$ = 1 ⇒ read

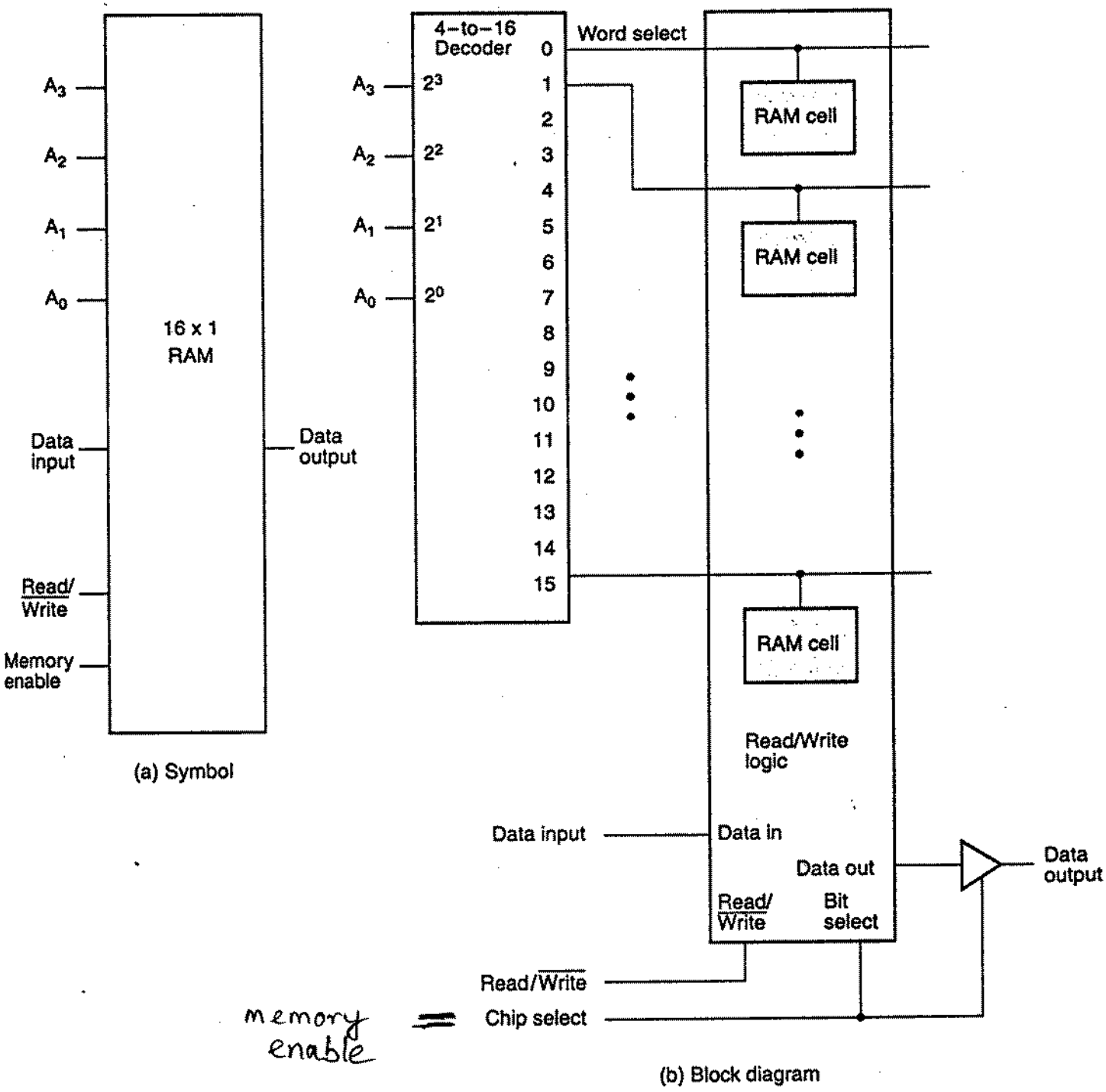


STRUCTURE OF A RAM CHIP

Control Inputs to a Memory Chip

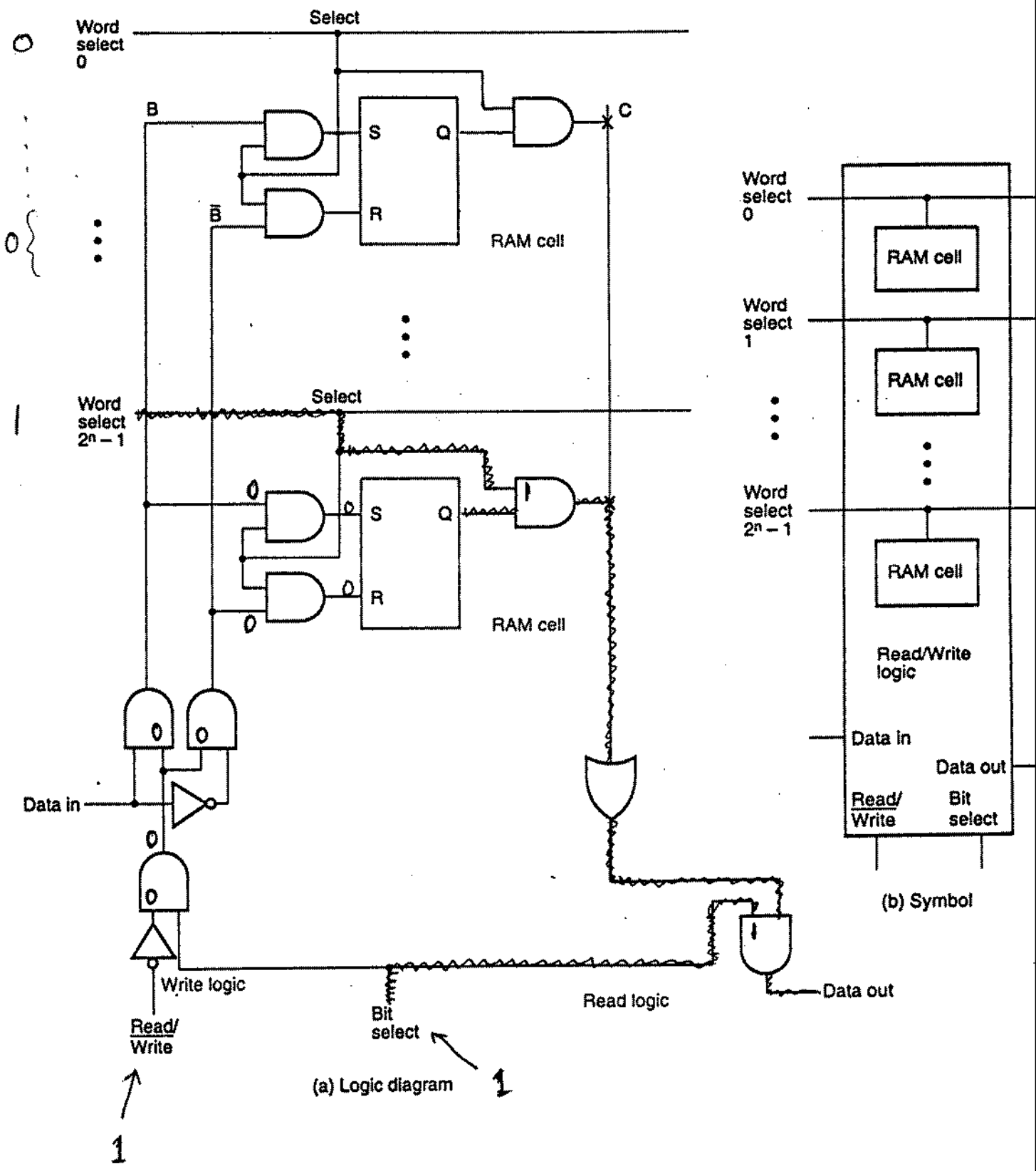
Chip select CS	Read/$\overline{\text{Write}}$ R/$\overline{\text{W}}$	Memory operation
0	×	None
1	0	Write to selected word
1	1	Read from selected word

word ≡ addressable location that contains n bits.

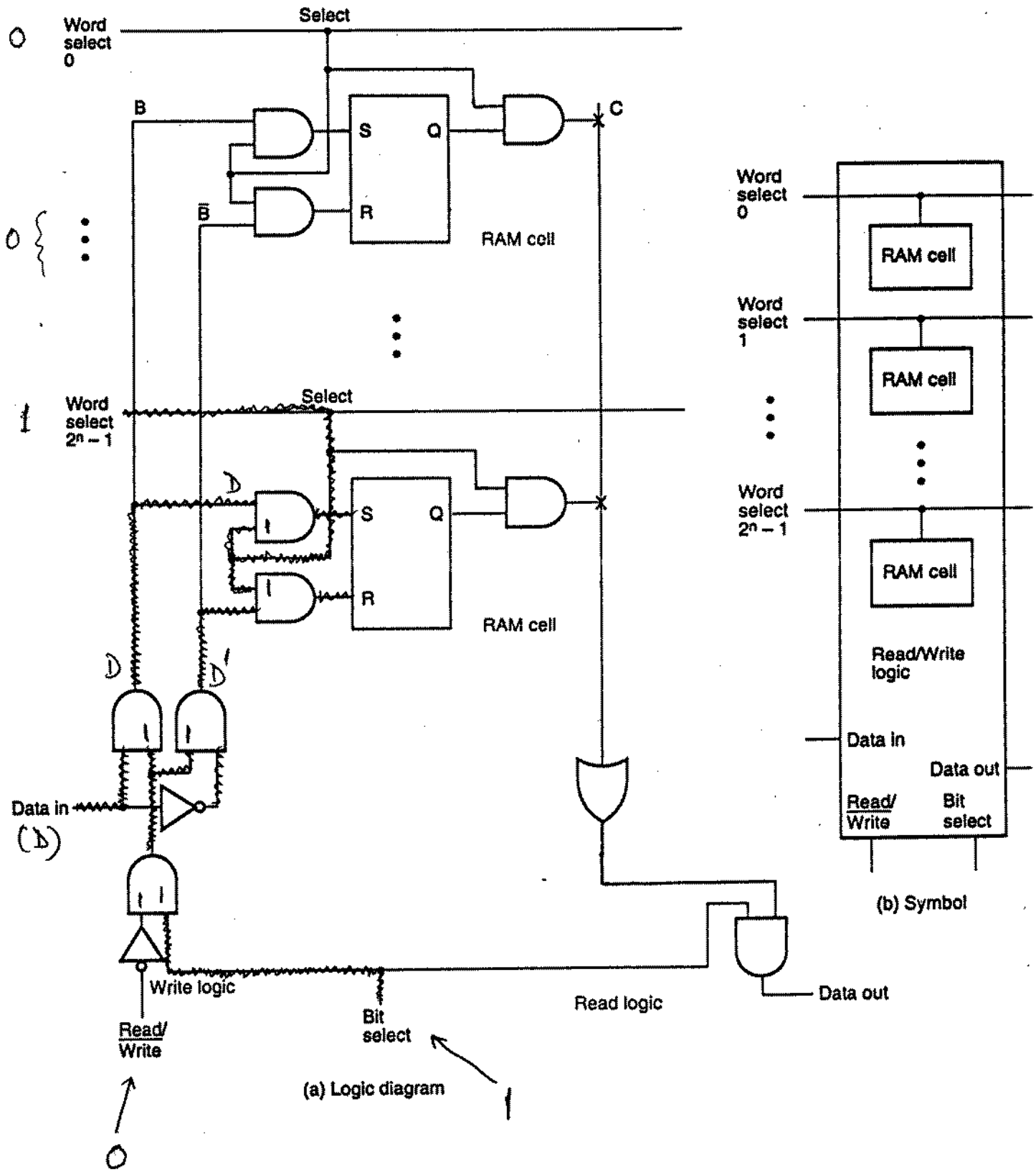


16-Word by 1-Bit RAM Chip

Read

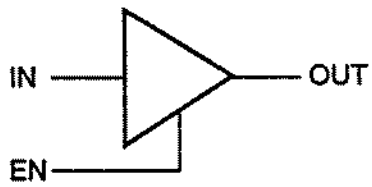

Word select 0
Select
B
$\bar{B}$
S
Q
R
C
RAM cell
Word select $2^n - 1$
Select
S
Q
R
RAM cell
Data in
Write logic
Read/ Write
Bit select
Read logic
Data out
(a) Logic diagram
Word select 0
RAM cell
Word select 1
RAM cell
Word select $2^n - 1$
RAM cell
Read/Write logic
Data in
Data out
Read/ Write
Bit select
(b) Symbol

Write


Word select 0
Select
B
$\bar{B}$
S
Q
R
C
RAM cell
Word select $2^n - 1$
Select
D
D'
Data in
(D)
Write logic
Read/ Write
Bit select
Read logic
Data out
(a) Logic diagram
Word select 0
Word select 1
Word select $2^n - 1$
RAM cell
Read/Write logic
Data in
Data out
Read/ Write
Bit select
(b) Symbol

Three-State Buffers

As the name implies, a three-state logic output exhibits three distinct states. Two of the states are the logic 1 and logic 0 of conventional logic. The third state is the *high-impedance* (Hi-*Z*) state. The high-impedance state behaves like an open circuit, which means that, looking back into the logic circuit, we would find that the output appears to be disconnected. Three-state outputs may appear on any logic block.



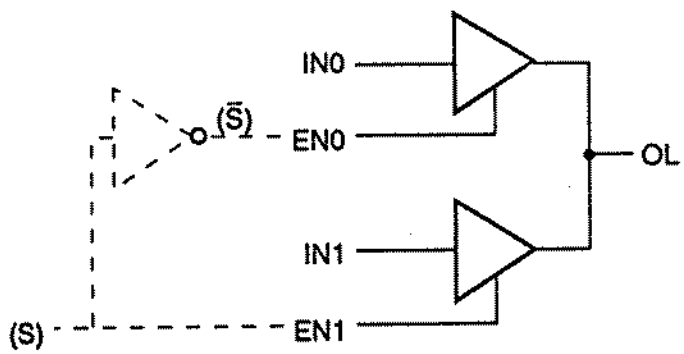
(a) Logic symbol

EN	IN	OUT
0	X	Hi-Z
1	0	0
1	1	1

(b) Truth table

Three-state Buffer

Allows construction of a multiplexer with an arbitrary inputs.



(a) Logic Diagram

EN1	EN0	IN1	IN0	OL
0	0	X	X	Hi-Z
(S) 0	($\bar{S}$) 1	X	0	0
0	1	X	1	1
1	0	0	X	0
1	0	1	X	1
1	1	0	0	0
1	1	1	1	1
1	1	0	1	
1	1	1	0	

(b) Truth table

Three-state Buffers Forming a Multiplexed Line OL

Example 16×1 RAM using 4 4×1 RAMs.
Which cell will be selected when $A_3 A_2 A_1 A_0 = 1011$?

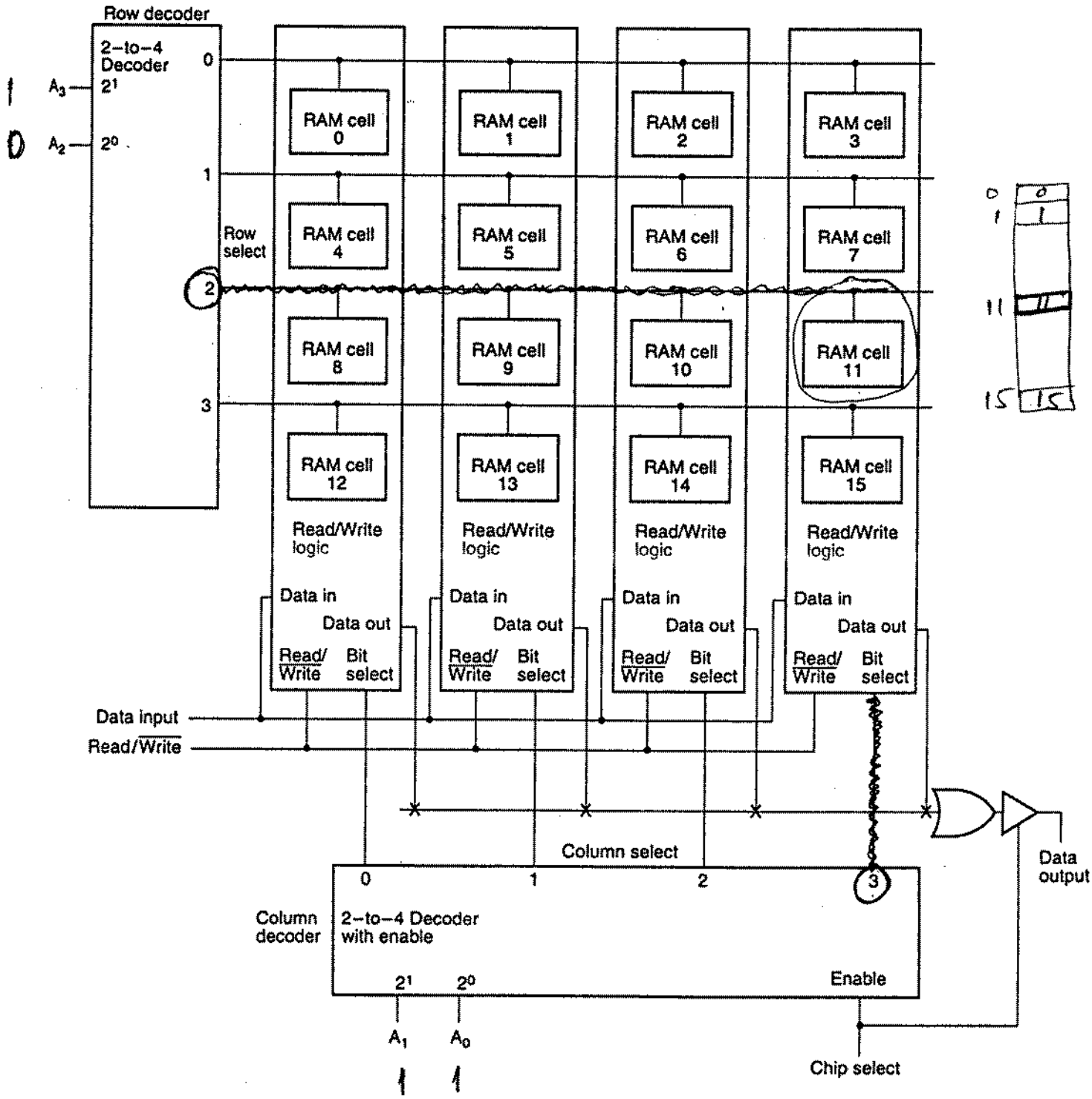


Diagram of a 16 × 1 RAM Using a 4 × 4 RAM Cell Array

Example 8 x 2 RAM using 4 4x1 RAMs

which cells will be selected if $A_2 A_1 A_0 = 101$?

0	0	1
1	2	3
5	10	11
7	14	15

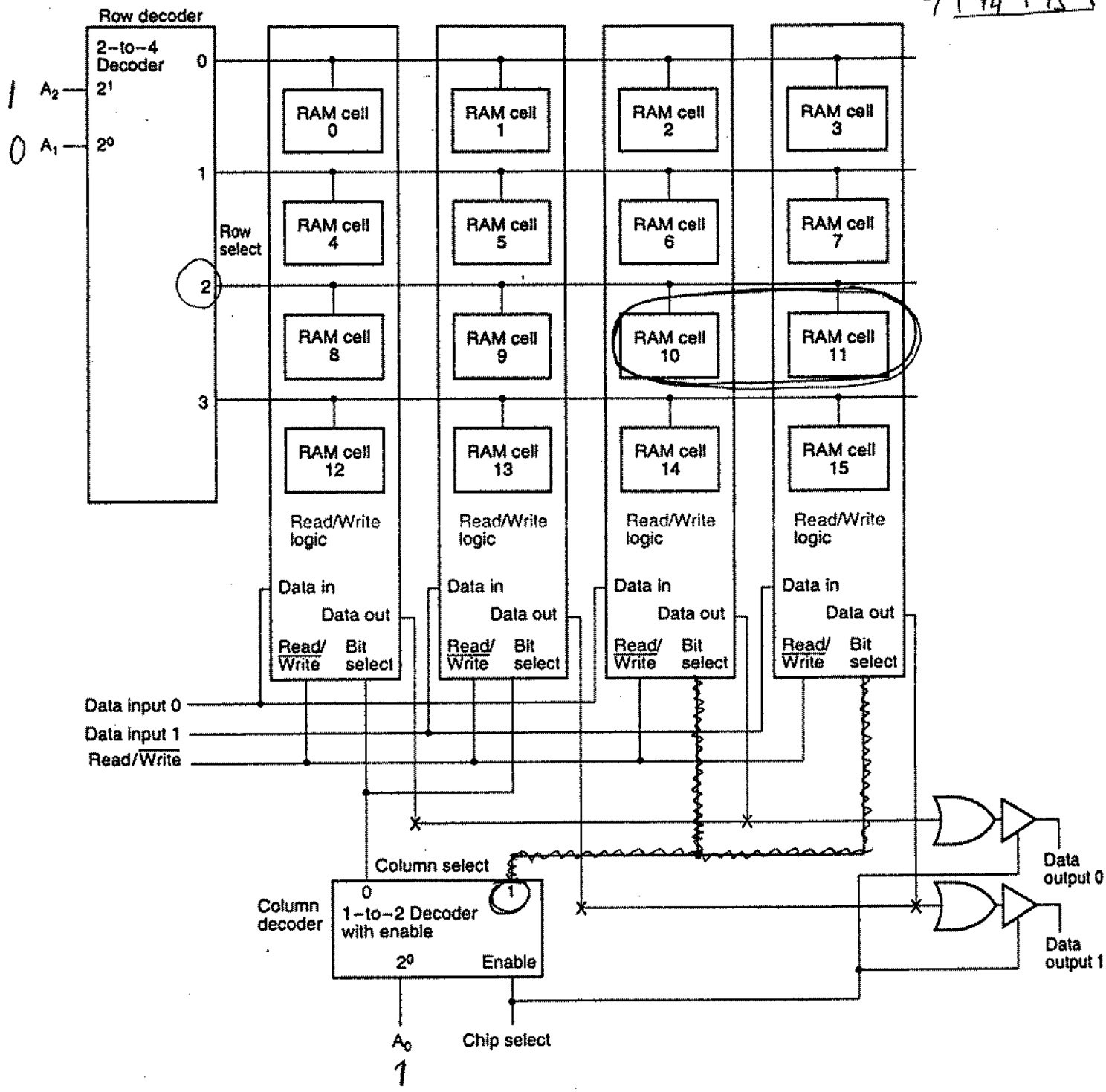
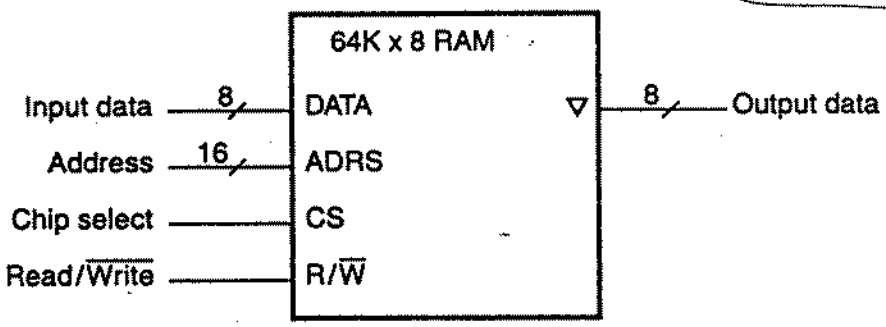


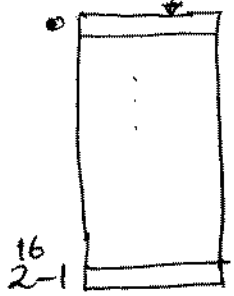
Diagram of an 8 × 2 RAM Using a 4 × 4 RAM Cell Array

ARRAY OF RAM CHIPS

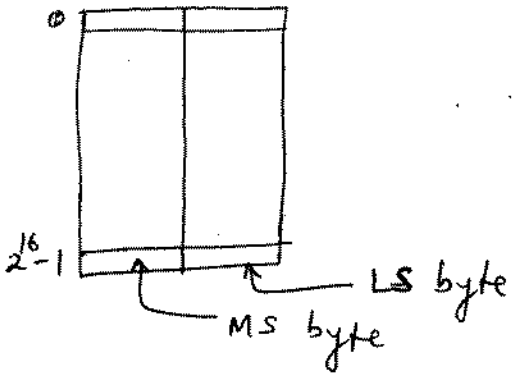
Basic element 64K x 8 RAM chips

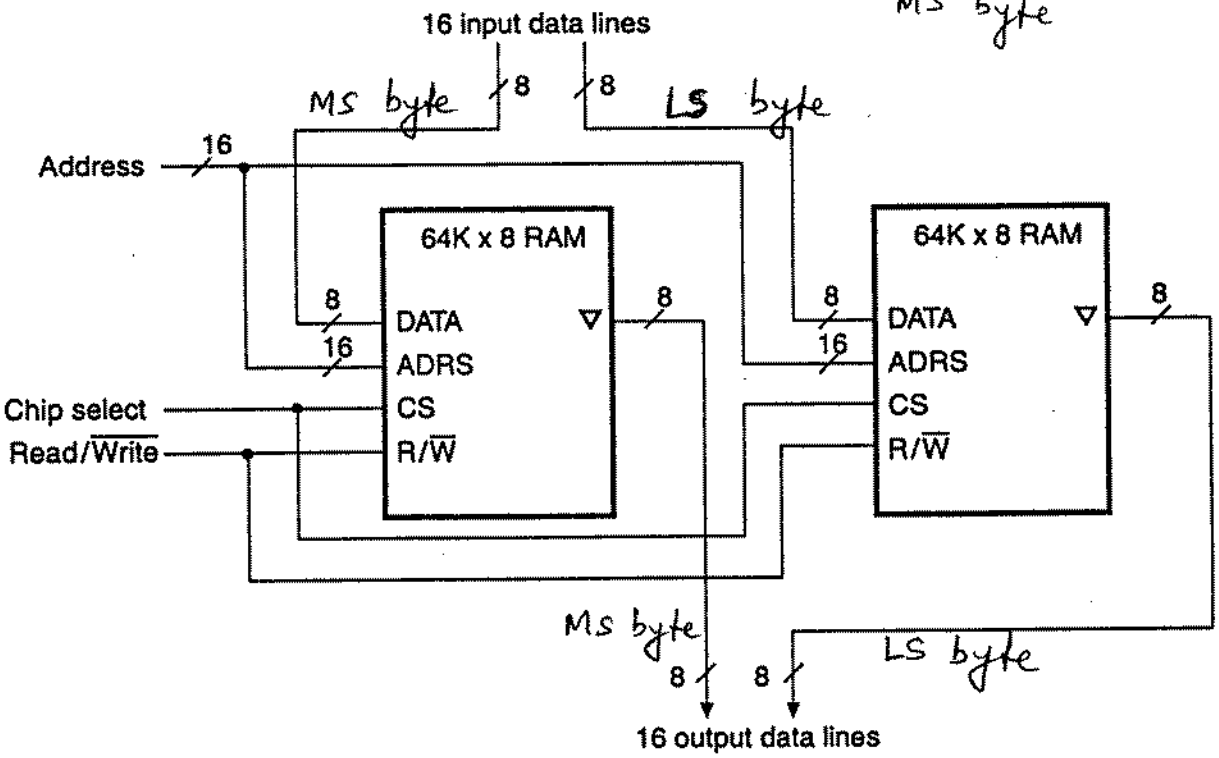
8 bits ≡ 1 byte





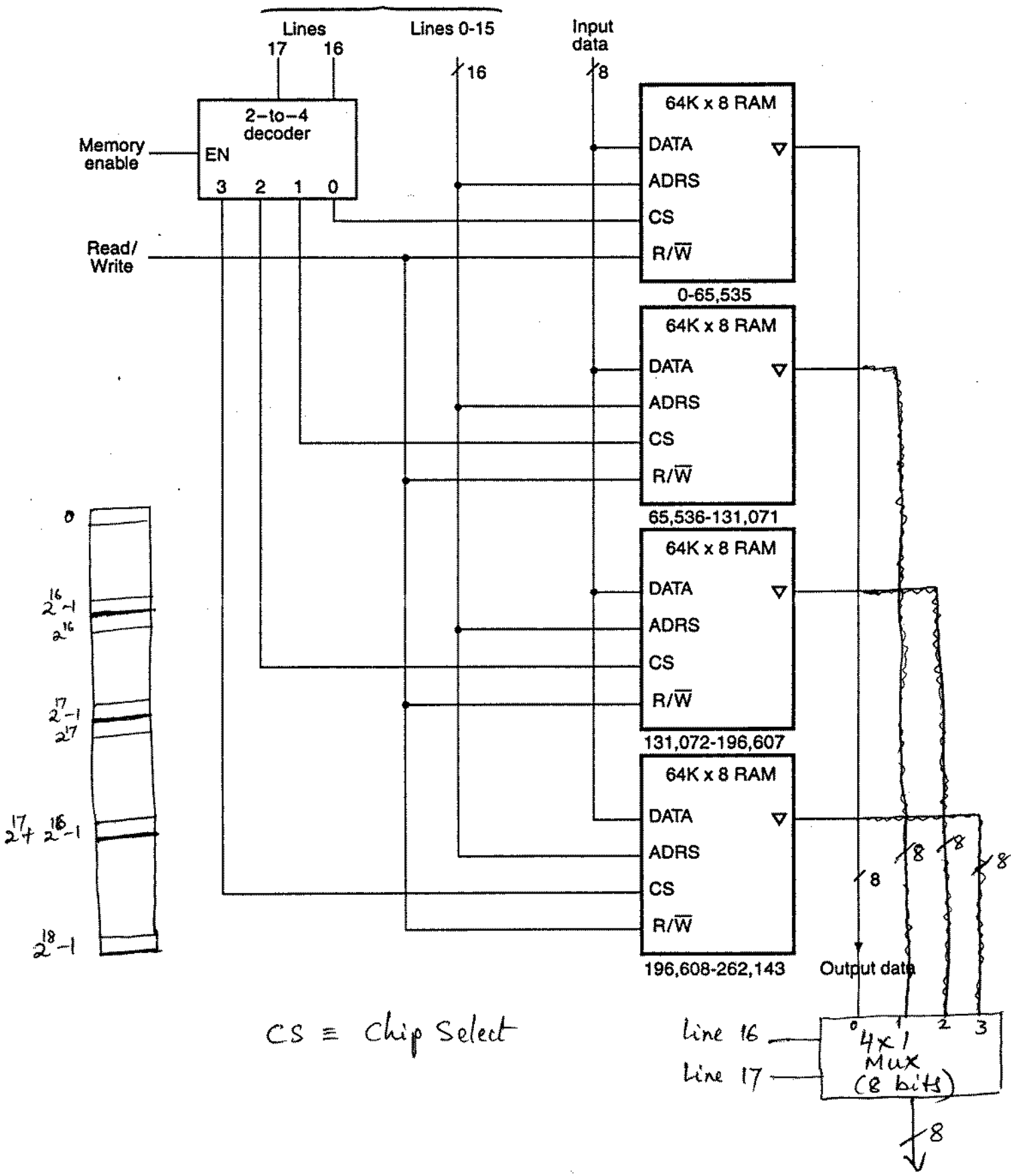
A) Construct 64K x 16 RAM



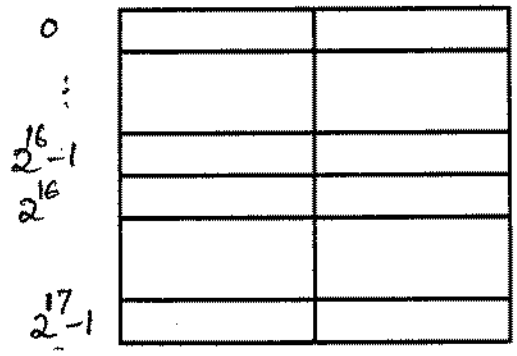


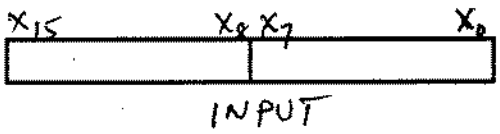
B) Construct a 256 K x 8 RAM

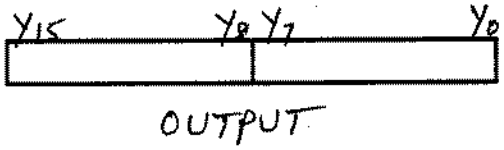
Address is 18 bits = 2 + 16 bits

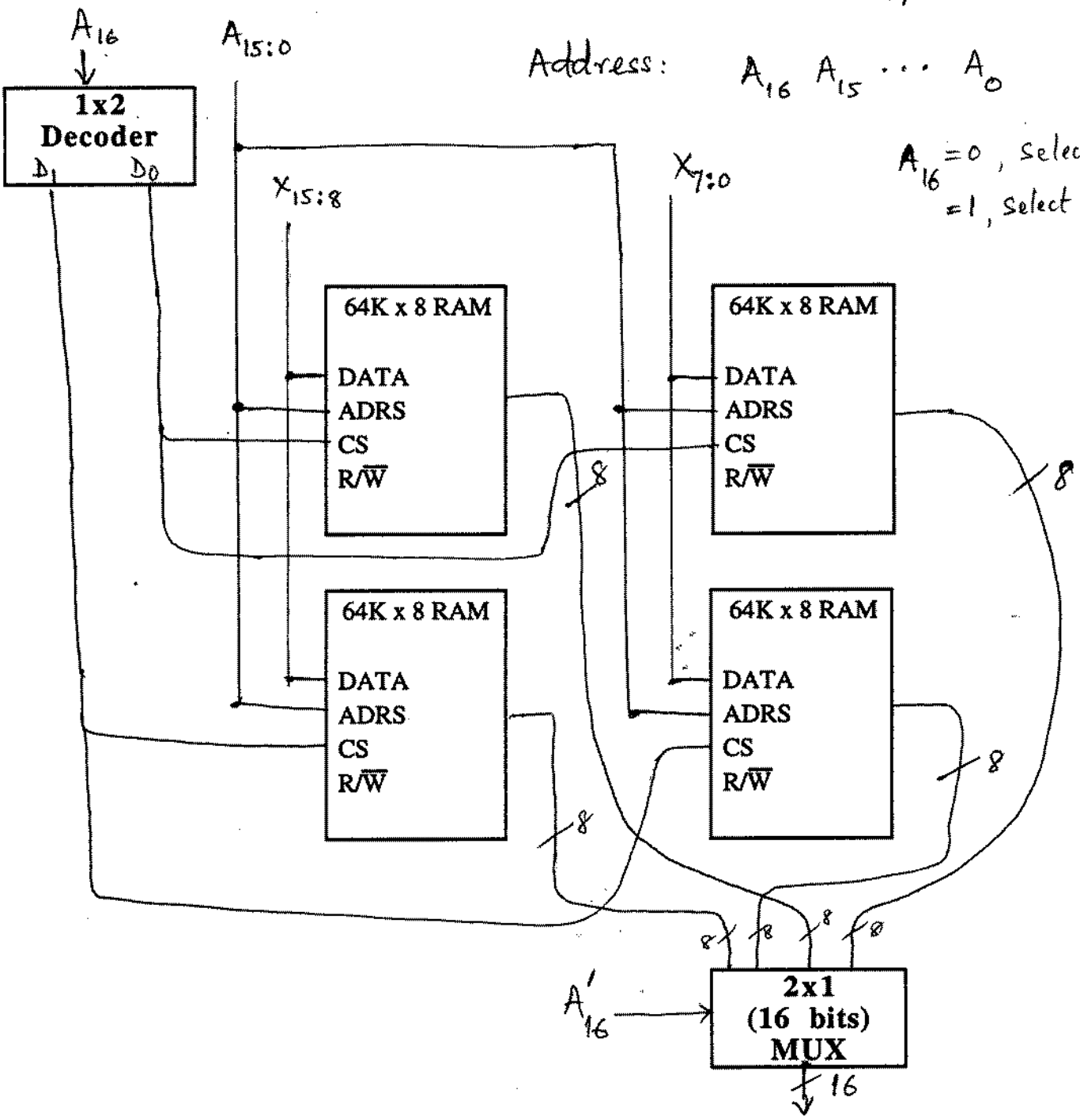


Example Construct 128K x 16 RAM using 64K x 8 RAMs







Address: $A_{16}\ A_{15} \cdots A_0$

$A_{16} = 0$, select top two
$= 1$, select bottom two