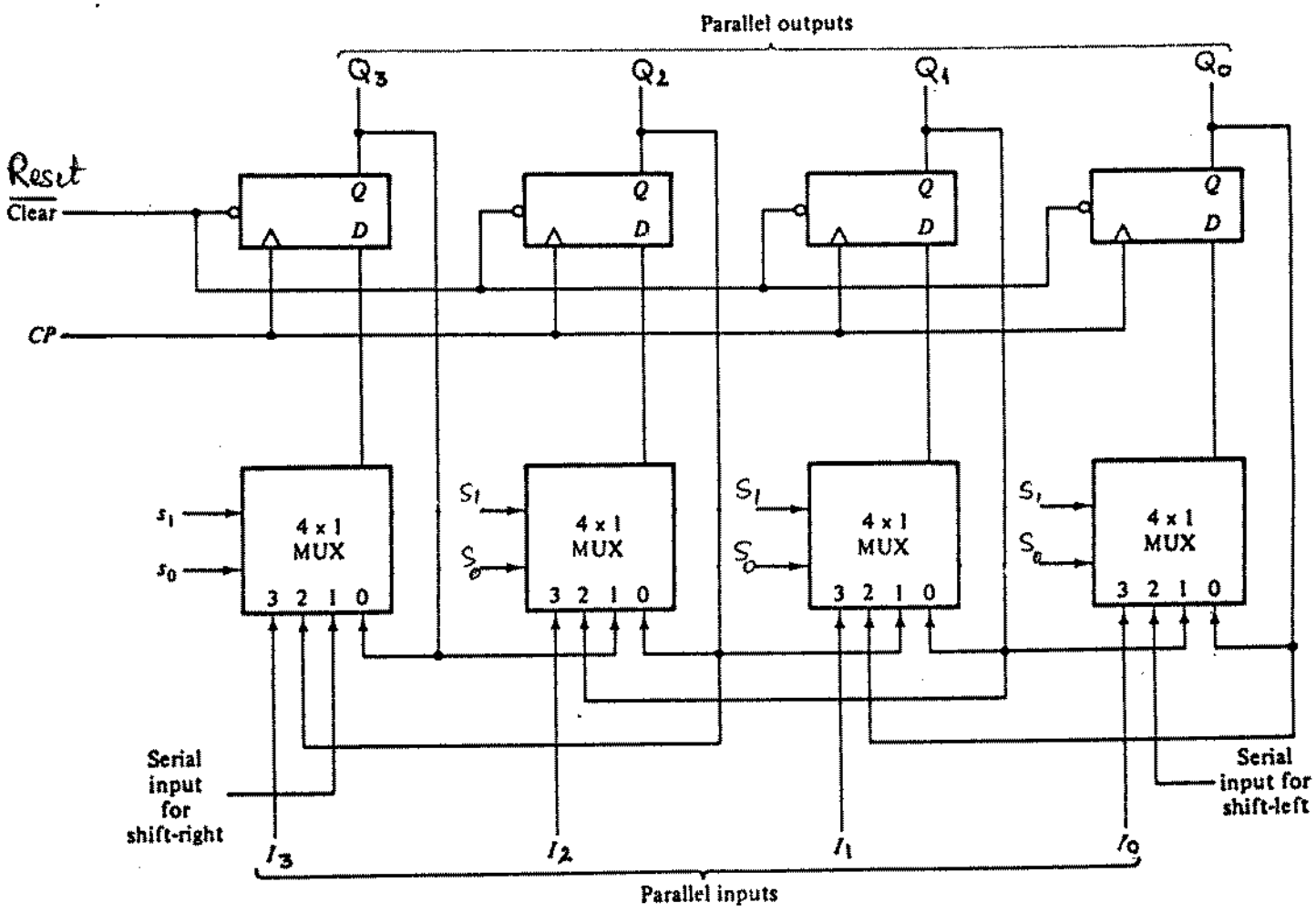
BIDIRECTIONAL SHIFT REGISTER WITH PARALLEL LOAD

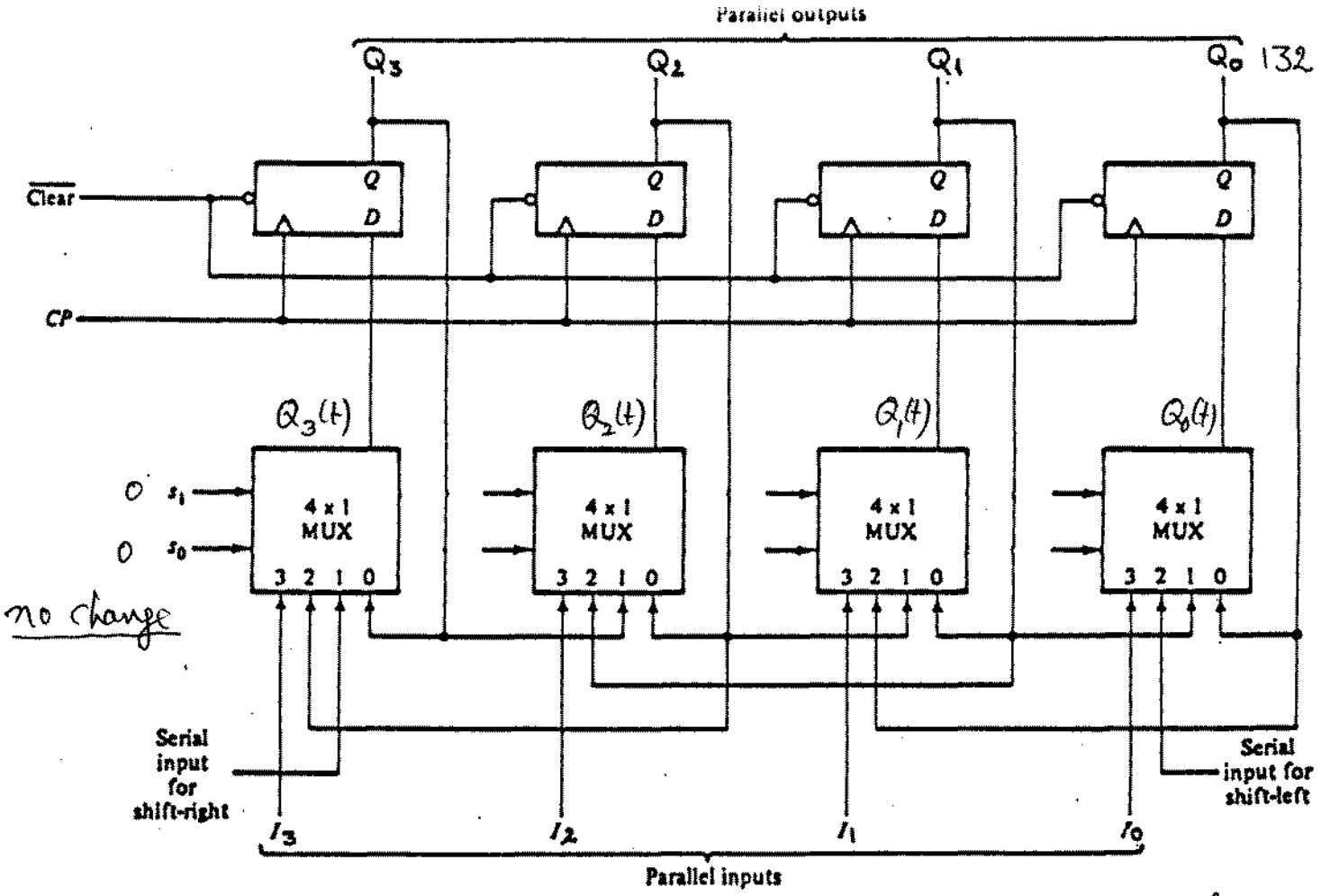
Function Table for the Register

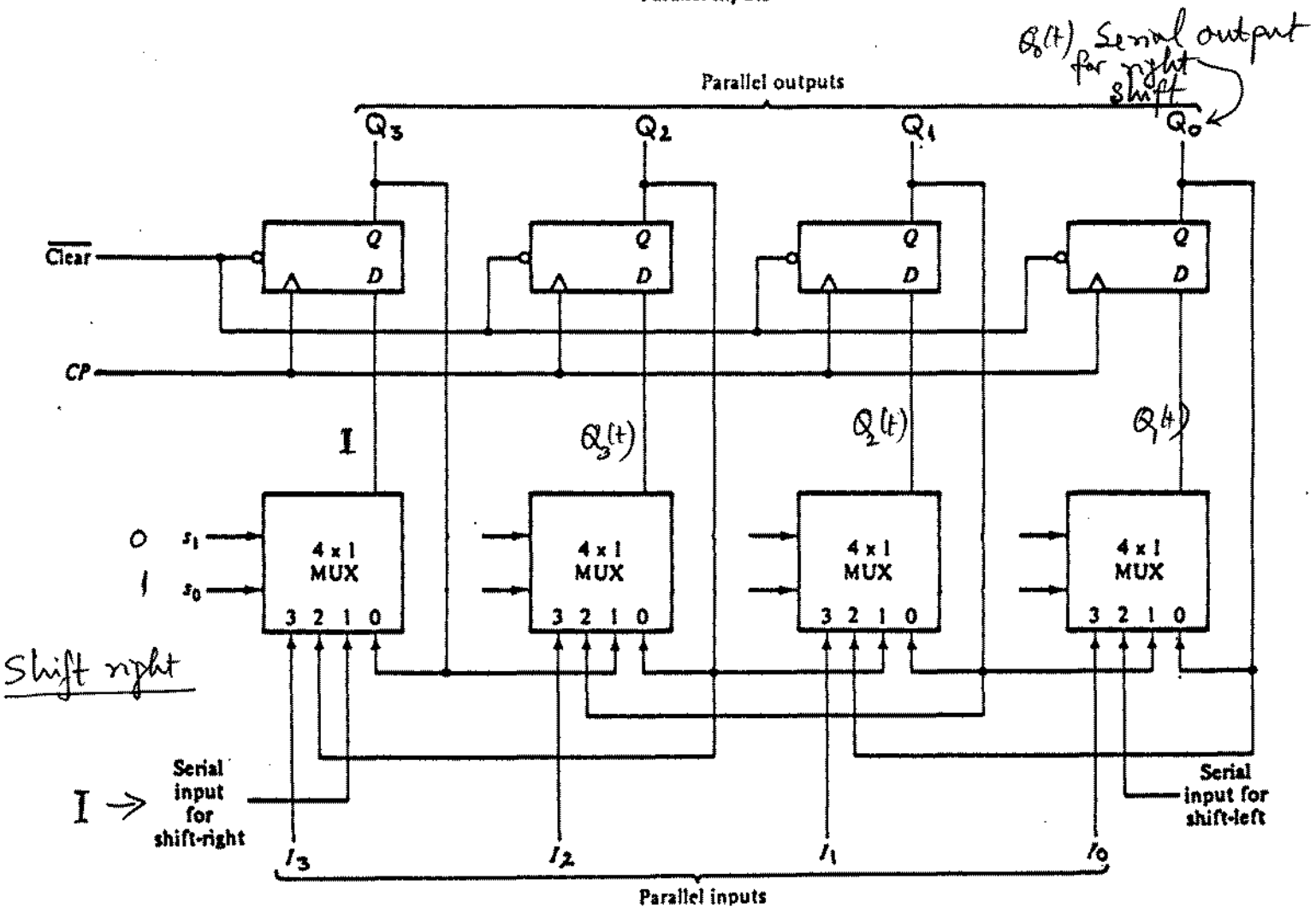
Mode Control		
s_1	s_0	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

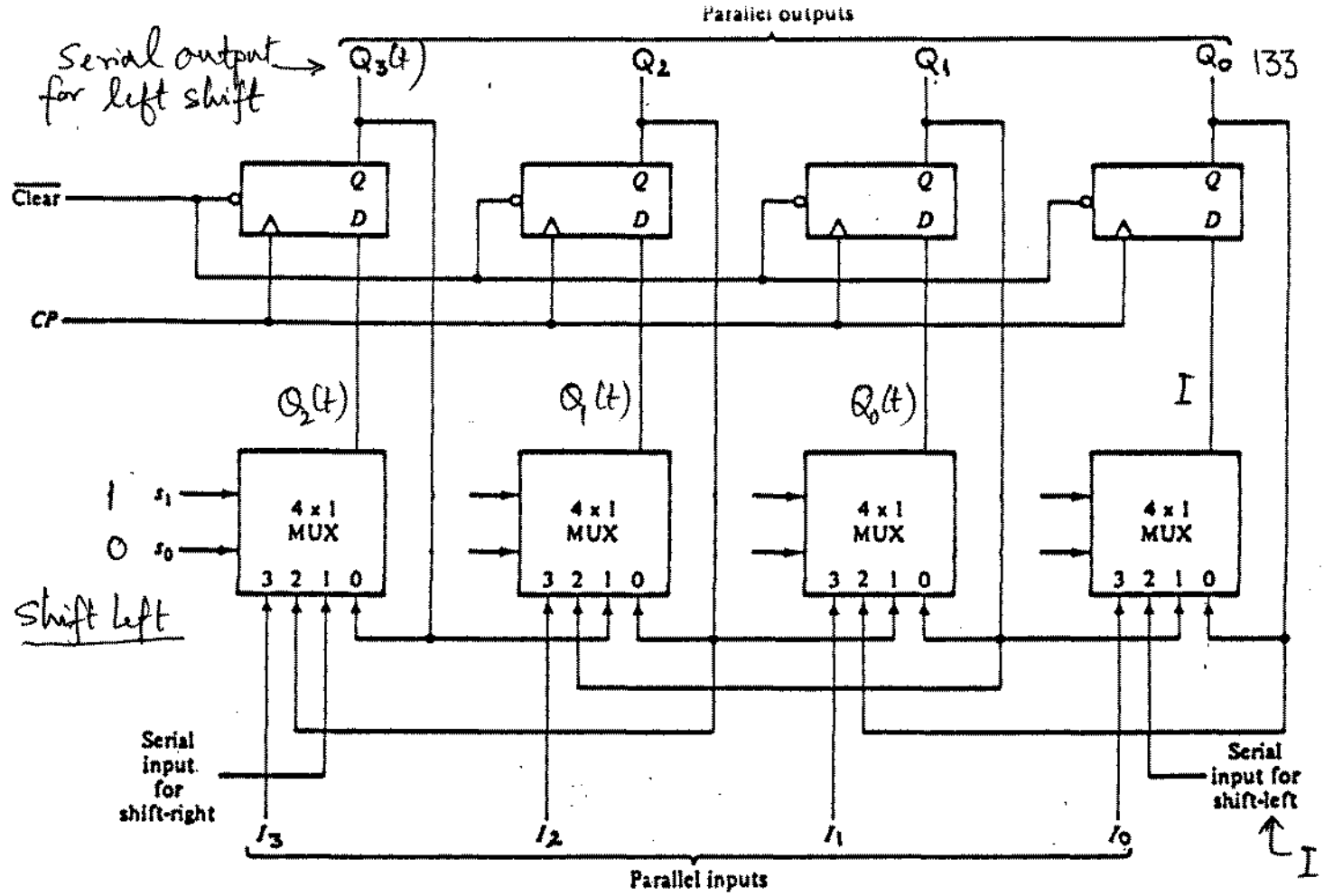
The diagram of a shift register that has all the capabilities listed above is shown below. It consists of four *D* flip-flops, although *RS* flip-flops could be used provided an inverter is inserted between the *S* and *R* terminals. The four multiplexers (MUX) are part of the register and are drawn here in block diagram form.

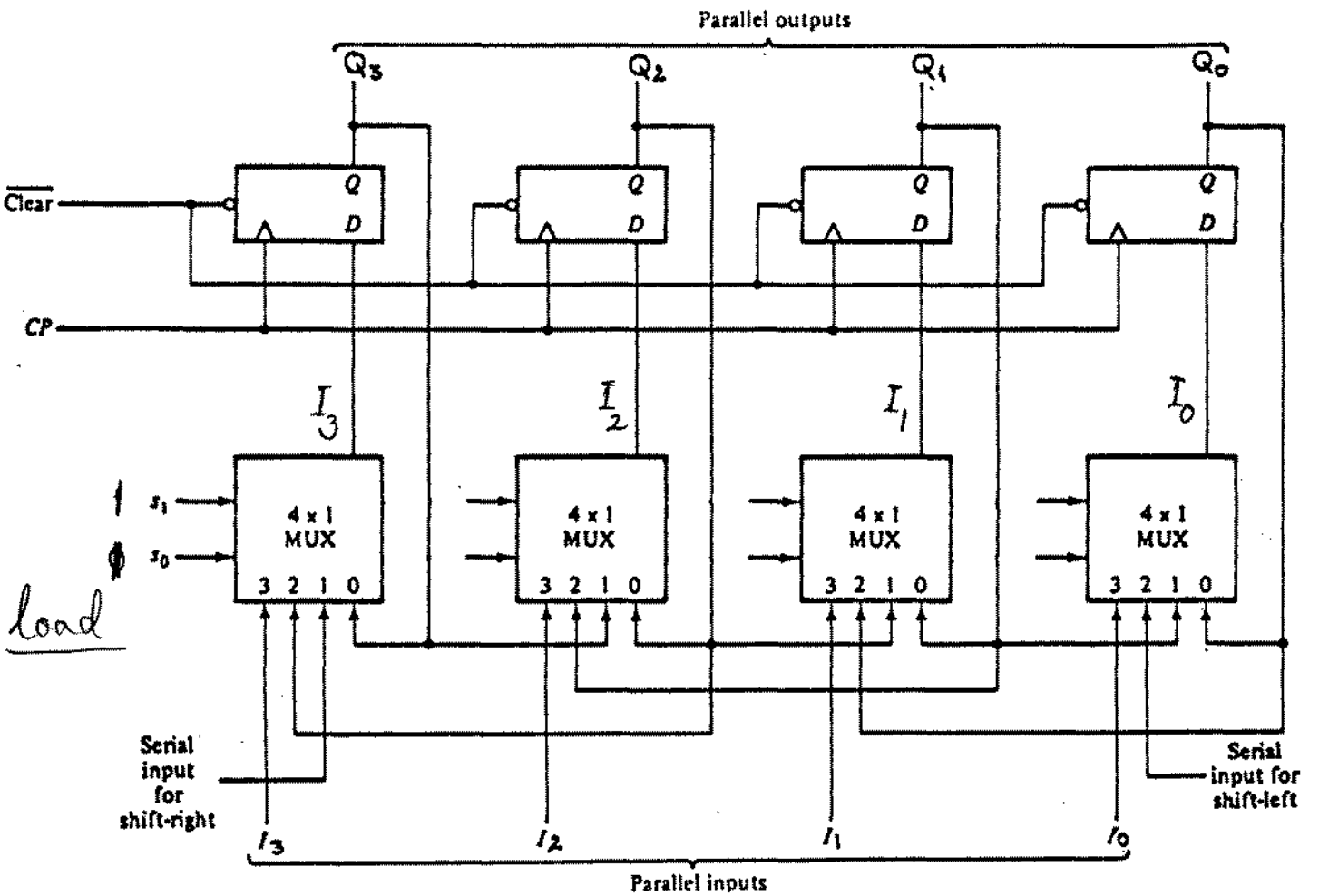
The four multiplexers have two common selection variables, s_1 and s_0. Input 0 in each MUX is selected when $s_1 s_0 = 00$, input 1 is selected when $s_1 s_0 = 01$, and similarly for the other two inputs to the multiplexers.




Parallel outputs
Q_3
Q_2
Q_1
Q_0
Clear
CP
Q
D
$Q_3(t)$
$Q_2(t)$
$Q_1(t)$
$Q_0(t)$
0 s_1
0 s_0
4 x 1 MUX
3 2 1 0
no change
Serial input for shift-right
Serial input for shift-left
I_3
I_2
I_1
I_0
Parallel inputs


$Q_0(t)$ Serial output for right shift
Parallel outputs
Q_3
Q_2
Q_1
Q_0
Clear
CP
Q
D
I
$Q_3(t)$
$Q_2(t)$
$Q_1(t)$
0 s_1
1 s_0
4 x 1 MUX
3 2 1 0
Shift right
I → Serial input for shift-right
Serial input for shift-left
I_3
I_2
I_1
I_0
Parallel inputs


Parallel outputs
Serial output for left shift
$Q_3(t)$
Q_2
Q_1
Q_0
Clear
CP
Q
D
$Q_2(t)$
$Q_1(t)$
$Q_0(t)$
I
1
0
s_1
s_0
4 x 1 MUX
3 2 1 0
Shift left
Serial input for shift-right
Serial input for shift-left
I_3
I_2
I_1
I_0
Parallel inputs


Parallel outputs
Q_3
Q_2
Q_1
Q_0
Clear
CP
Q
D
I_3
I_2
I_1
I_0
1
0
s_1
s_0
4 x 1 MUX
3 2 1 0
load
Serial input for shift-right
Serial input for shift-left
I_3
I_2
I_1
I_0
Parallel inputs

Section 5.4 – 5.6

COUNTER

A SEQUENTIAL CIRCUIT (a cascade of JK or T FF's)
THAT GOES THROUGH A PREDETERMINED SEQUENCE OF STATES

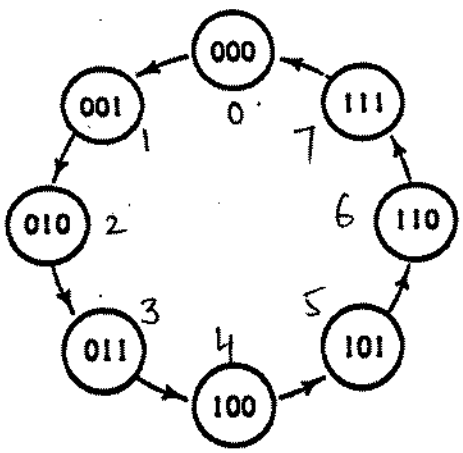
A) RIPPLE COUNTER

A counter in which CP inputs of all FF's (except the 1st FF) are triggered not by incoming clock pulses but rather by state transitions that occur in the preceding FF's

B) SYNCHRONOUS COUNTER

A counter in which CP inputs of all FF's are triggered by incoming clock pulses

e.g., 3-BIT BINARY SYNCHRONOUS COUNTER (using T FFs)

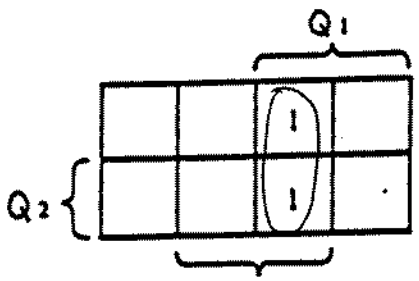


State diagram of a 3-bit binary counter

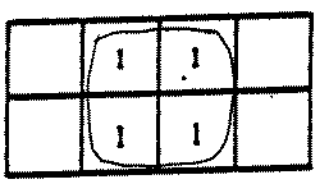
Excitation Table for 3-Bit Counter

Present State			Next State			Flip-Flop Inputs		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	TQ_2	TQ_1	TQ_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

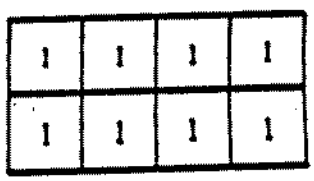
$Q(t+1) = Q'(t)$ if $T=1$



$TQ_2 = Q_1Q_0$

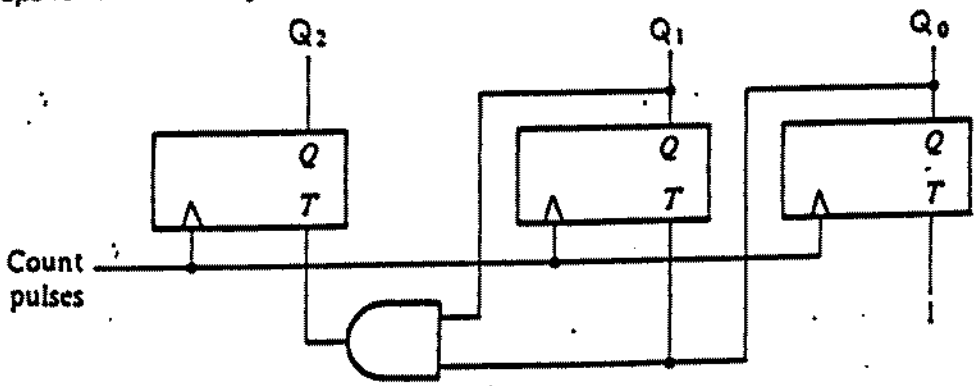


$TQ_1 = Q_0$



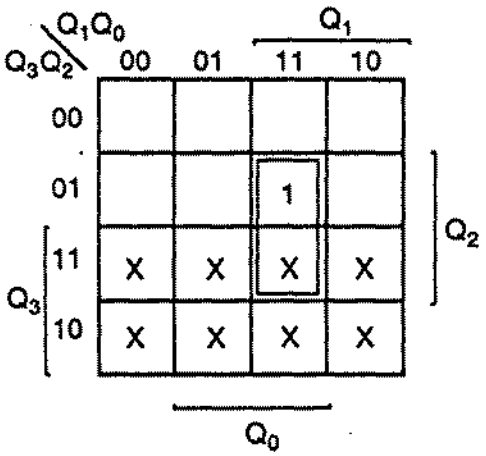
$TQ_0 = 1$

Maps for a 3-bit binary counter

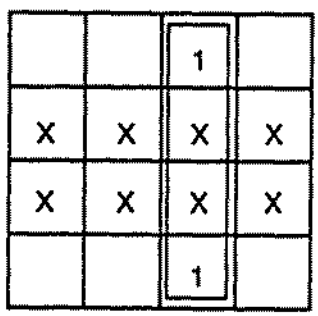


e.g., 4-BIT BINARY SYNCHRONOUS COUNTER (using JK FFs)
Count from 0 to 2^4-1

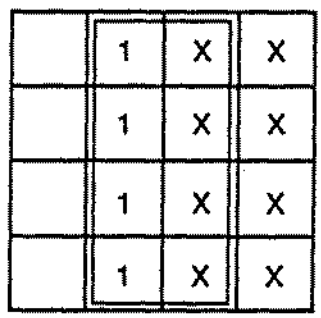
Present state				Next state				Flip-flop inputs							
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	J_{Q3}	K_{Q3}	J_{Q2}	K_{Q2}	J_{Q1}	K_{Q1}	J_{Q0}	K_{Q0}
0	0	0	0	0	0	0	1	0	×	0	×	0	×	1	×
0	0	0	1	0	0	1	0	0	×	0	×	1	×	×	1
0	0	1	0	0	0	1	1	0	×	0	×	×	0	1	×
0	0	1	1	0	1	0	0	0	×	1	×	×	1	×	1
0	1	0	0	0	1	0	1	0	×	×	0	0	×	1	×
0	1	0	1	0	1	1	0	0	×	×	0	1	×	×	1
0	1	1	0	0	1	1	1	0	×	×	0	×	0	1	×
0	1	1	1	1	0	0	0	1	×	×	1	×	1	×	1
1	0	0	0	1	0	0	1	×	0	0	×	0	×	1	×
1	0	0	1	1	0	1	0	×	0	0	×	1	×	×	1
1	0	1	0	1	0	1	1	×	0	0	×	×	0	1	×
1	0	1	1	1	1	0	0	×	0	1	×	×	1	×	1
1	1	0	0	1	1	0	1	×	0	×	0	0	×	1	×
1	1	0	1	1	1	1	0	×	0	×	0	1	×	×	1
1	1	1	0	1	1	1	1	×	0	×	0	×	0	1	×
1	1	1	1	0	0	0	0	×	1	×	1	×	1	×	1



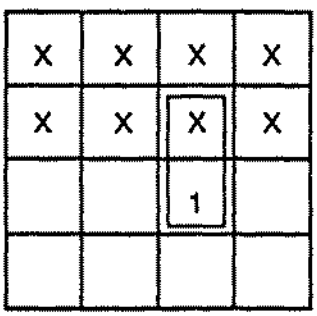
$J_{Q3} = Q_0Q_1Q_2$



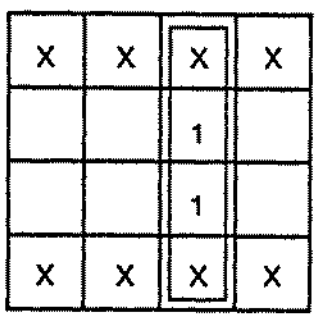
$J_{Q2} = Q_0Q_1$



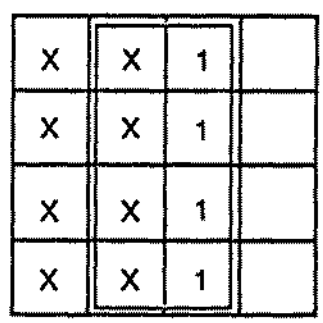
$J_{Q1} = Q_0$



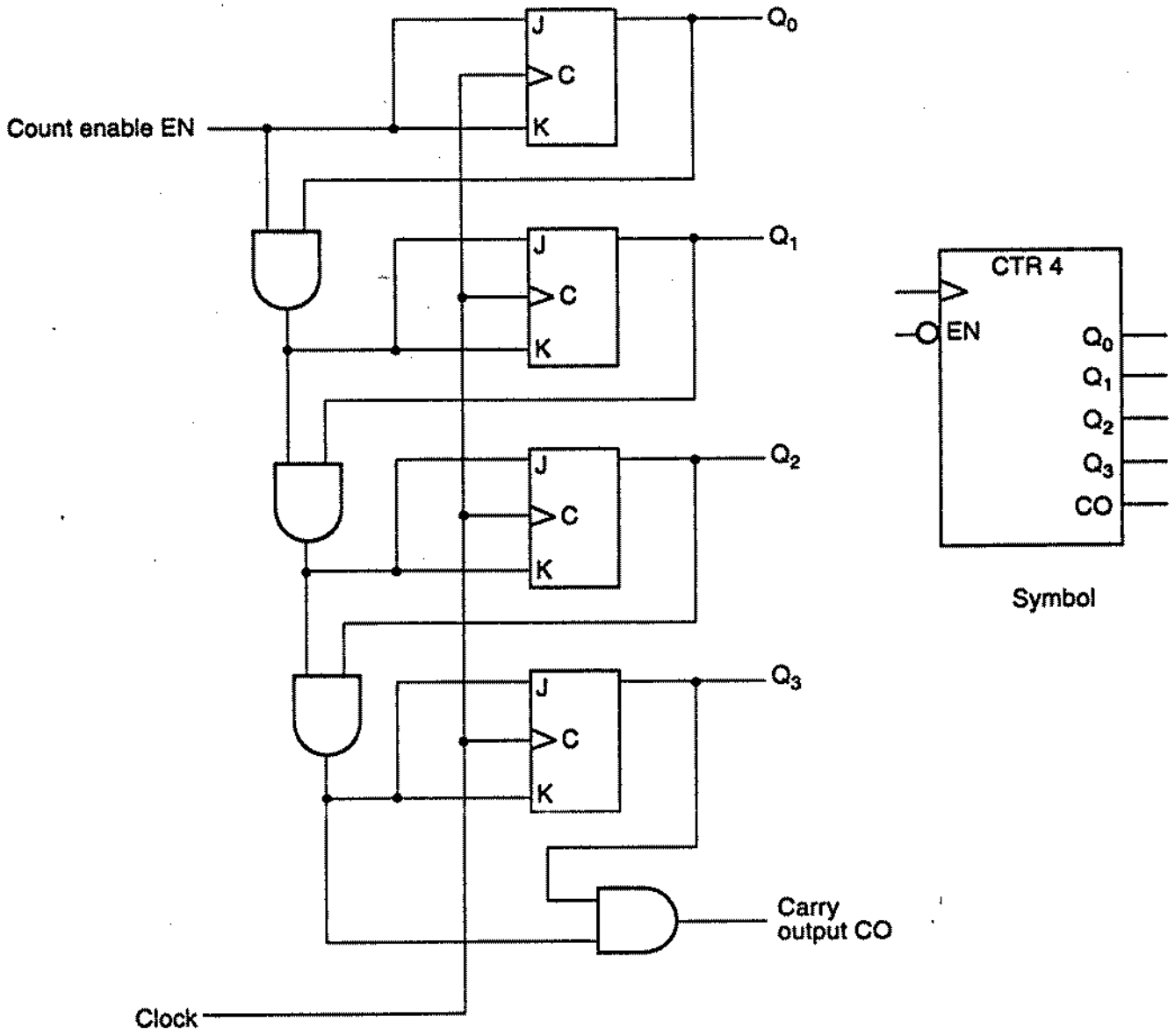
$K_{Q3} = Q_0Q_1Q_2$



$K_{Q2} = Q_0Q_1$



$K_{Q1} = Q_0$



$$J_{Q0} = K_{Q0} = EN$$

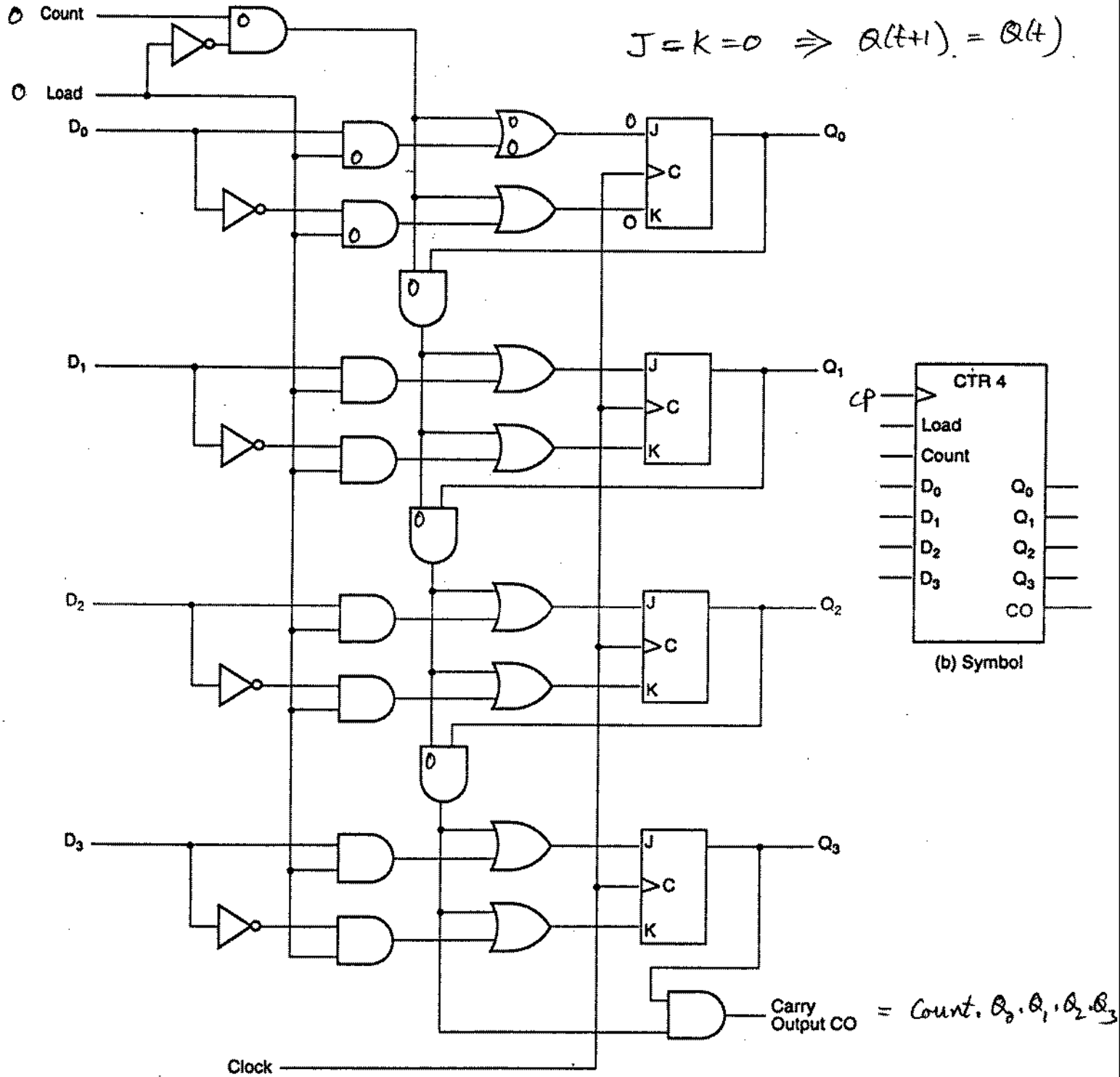
$$J_{Q1} = K_{Q1} = Q_0 \cdot EN$$

$$J_{Q2} = K_{Q2} = Q_0 \cdot Q_1 \cdot EN$$

$$J_{Q3} = K_{Q3} = Q_0 \cdot Q_1 \cdot Q_2 \cdot EN$$

When $EN = 0$, all J and K inputs are equal to 0, and the flip-flops remain in the same state, even in the presence of clock pulses. When $EN = 1$, the first input equation becomes $J_{Q0} = K_{Q0} = 1$, and the other input equations reduce to the equations derived.

e.g., BINARY SYNCHRONOUS COUNTER WITH PARALLEL LOAD



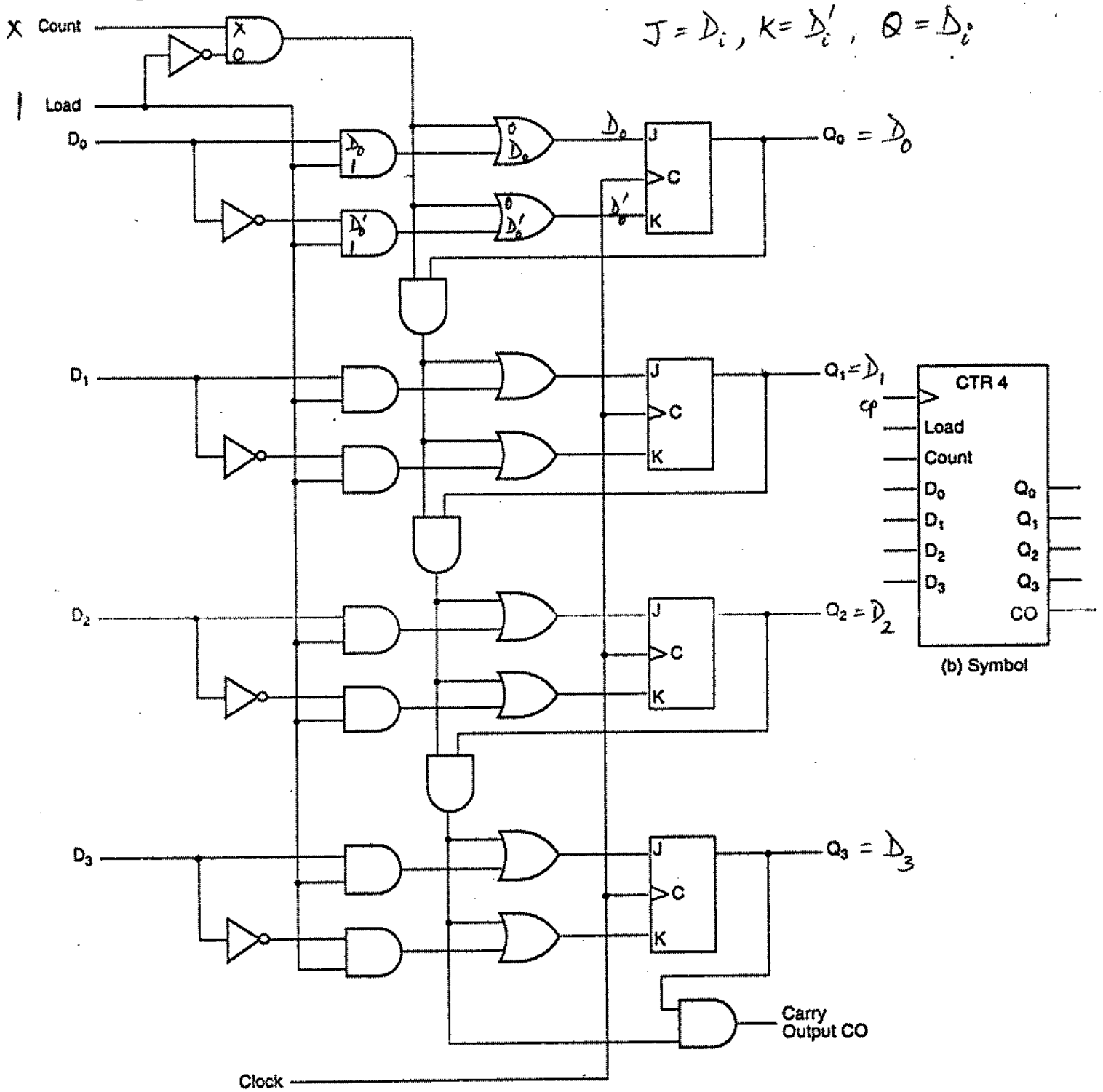
(a) Logic diagram

(b) Symbol

Load	Count	Operation
0	0	No change
0	1	Count next binary state
1	×	Load inputs

e.g., BINARY SYNCHRONOUS COUNTER WITH PARALLEL LOAD

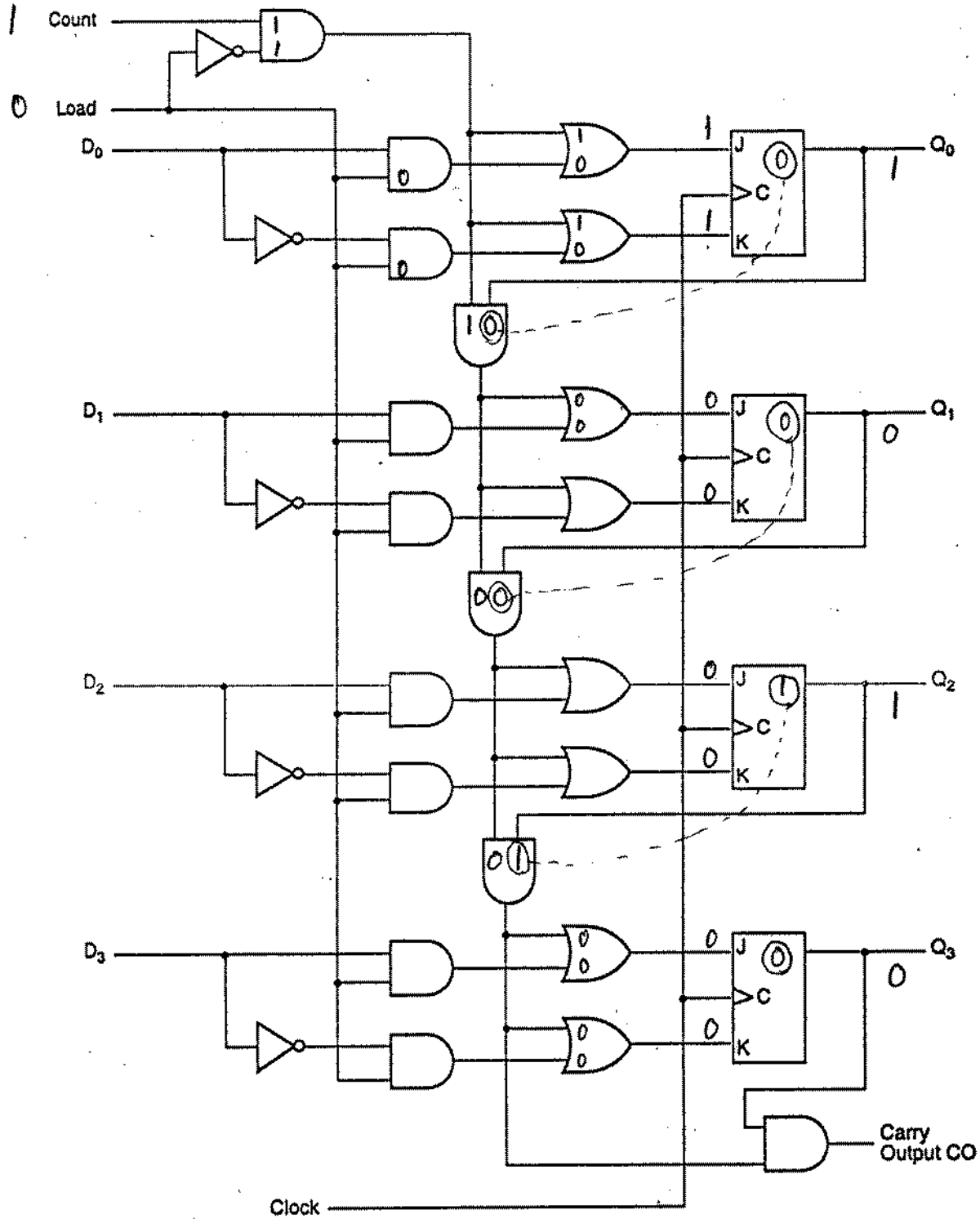
$J = D_i$, $K = D_i'$, $Q = D_i$



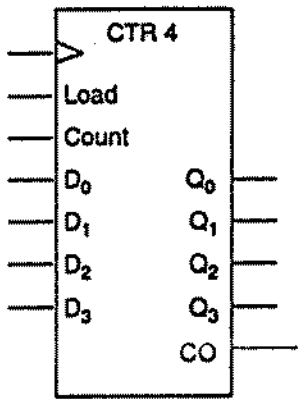
(a) Logic diagram

Load	Count	Operation
0	0	No change
0	1	Count next binary state
→ 1	×	Load inputs

e.g., BINARY SYNCHRONOUS COUNTER WITH PARALLEL LOAD



(a) Logic diagram

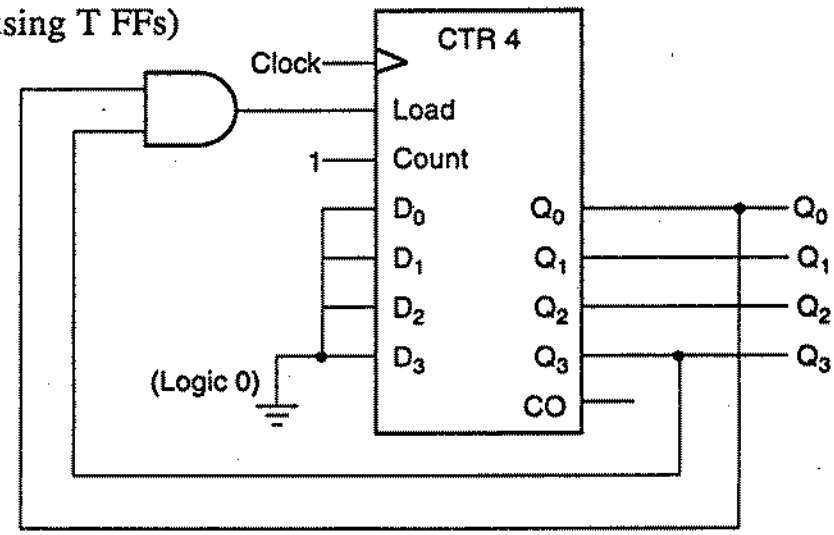


(b) Symbol

Load	Count	Operation
0	0	No change
→ 0	1	Count next binary state
1	×	Load inputs

Counter Modulo 10

e.g., BCD COUNTER (using T FFs)
counts from 0 to 9



State Table and Flip-Flop Inputs for BCD Counter

Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	Y	T_{Q8}	T_{Q4}	T_{Q2}	T_{Q1}
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

The flip-flop input equations are obtained from the flip-flop inputs listed in the table and can be simplified by means of maps. The unused states for minterms 1010 through 1111 are taken as don't-care conditions. The simplified input equations for the BCD counter are:

$$T_{Q1} = 1$$

$$T_{Q2} = Q_1\overline{Q}_8$$

$$T_{Q4} = Q_1Q_2$$

$$T_{Q8} = Q_1Q_8 + Q_1Q_2Q_4$$

$$Y = Q_1Q_8$$

The circuit can be drawn with four T flip-flops, four AND gates, and one OR gate.

COUNTERS WITH ARBITRARY COUNT SEQUENCES

e.g., Count sequence 0 1 2 4 5 6 and repeat

State Table and Flip-Flop Inputs for Counter

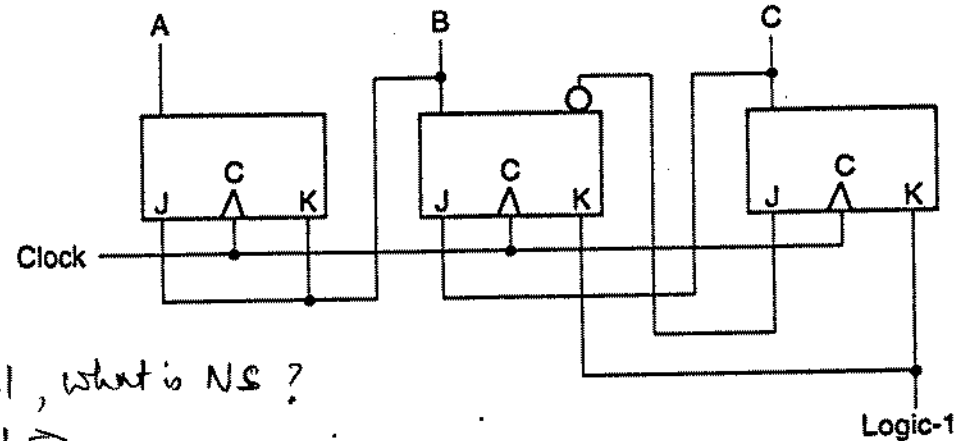
Present State			Next State			Flip-Flop Inputs					
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	×	0	×	1	×
0	0	1	0	1	0	0	×	1	×	×	1
0	1	0	1	0	0	1	×	×	1	0	×
1	0	0	1	0	1	×	0	0	×	1	×
1	0	1	1	1	0	×	0	1	×	×	1
1	1	0	0	0	0	×	1	×	1	0	×

{ don't care states }

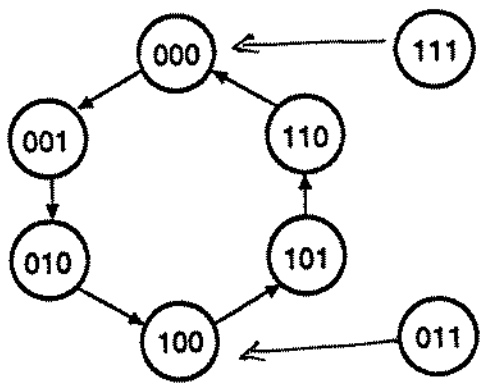
$J_A = B$ $\quad K_A = B$

$J_B = C$ $\quad K_B = 1$

$J_C = \overline{B}$ $\quad K_C = 1$



(a) Logic diagram



(b) State diagram

If PS = 011, what is NS?

$J_A = 1, K_A = 1 \Rightarrow$

$A(t+1) = 1$

$J_B = 1, K_B = 1 \Rightarrow$

$B(t+1) = 0$

$J_C = 0, K_C = 1 \Rightarrow$

$C(t+1) = 0$

$\therefore$ NS = 100

If PS = 111, what is NS?

$J_A = K_A = 1 \Rightarrow$

$A(t+1) = 0$

$J_B = 1, K_B = 1 \Rightarrow$

$B(t+1) = 0$

$J_C = 0, K_C = 1 \Rightarrow$

$C(t+1) = 0$

$\therefore$ NS = 000