REGISTER

A SEQUENTIAL CIRCUIT WHICH CONSISTS OF A GROUP OF FF'S AND (POSSIBLY) EXTERNAL GATES CONTROLLING THE FF INPUTS

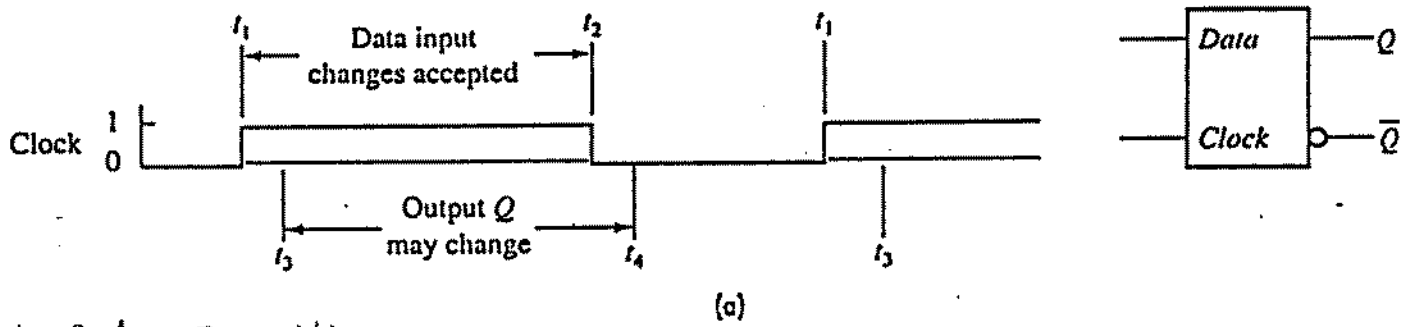
WHERE

FF'S HOLD BINARY INFO AND
EXTERNAL GATES CONTROL WHEN & HOW NEW BINARY INFO IS PUT INTO FF'S

* **(THE CONTENT OF A REGISTER = WORD** = BIT STREAM STORED IN FF'S)
* **(THE LENGTH OF A REGISTER = WORD LENGTH** = # OF FF'S IN A REGISTER)

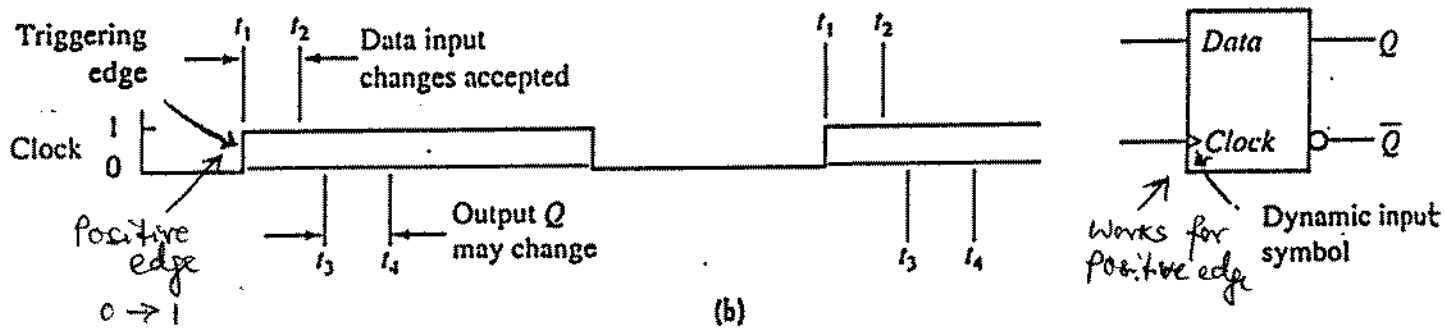
* ALL REGISTERS (EXCEPT GATED LATCHES) ARE BUILT BY USING FF'S THAT ARE SENSITIVE TO **PULSE TRANSITION** RATHER THAN TO **PULSE DURATION**

(A) Pulse Duration

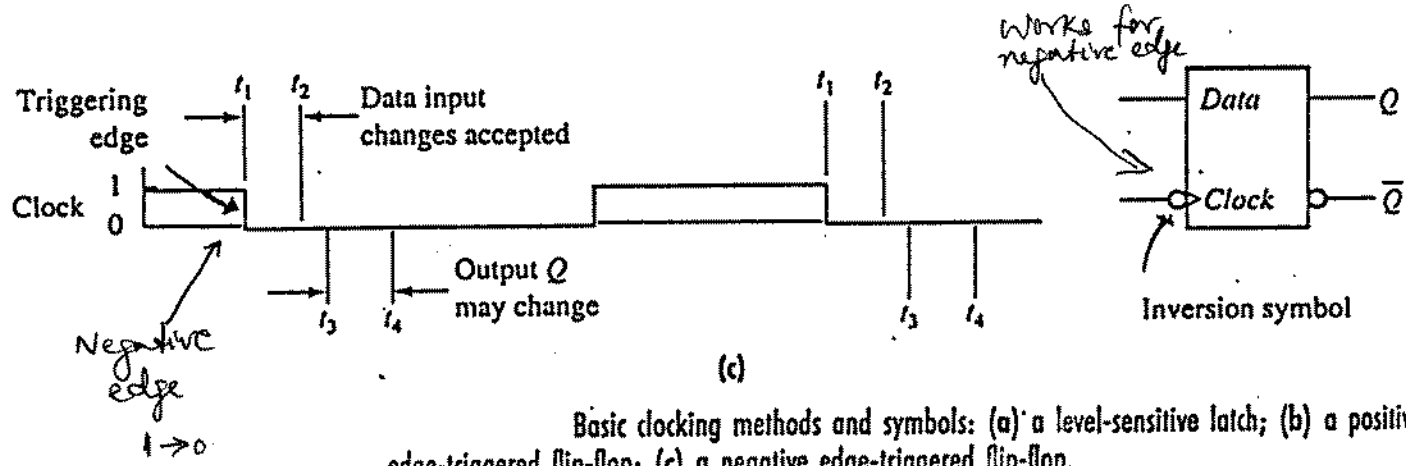


(a)

(B) Pulse Transition



(b)



(c)

Basic clocking methods and symbols: (a) a level-sensitive latch; (b) a positive edge-triggered flip-flop; (c) a negative edge-triggered flip-flop.

* THE TRANSFER OF NEW BINARY INFO INTO A REGISTER IS CALLED **LOADING**

* **SERIAL LOAD (TRANSFER IN SERIAL MODE)**
TRANSFER OF NEW BINARY INFO INTO A REGISTER BIT BY BIT
(# OF CLOCK PULSES NEEDED TO LOAD THE REGISTER = # OF FF'S IN THE REGISTER)

e.g., Let A and B be two n-bit registers

$A_n \cdots A_2A_1$ ---> $B_n \cdots B_2B_1$ 1 bit / pulse

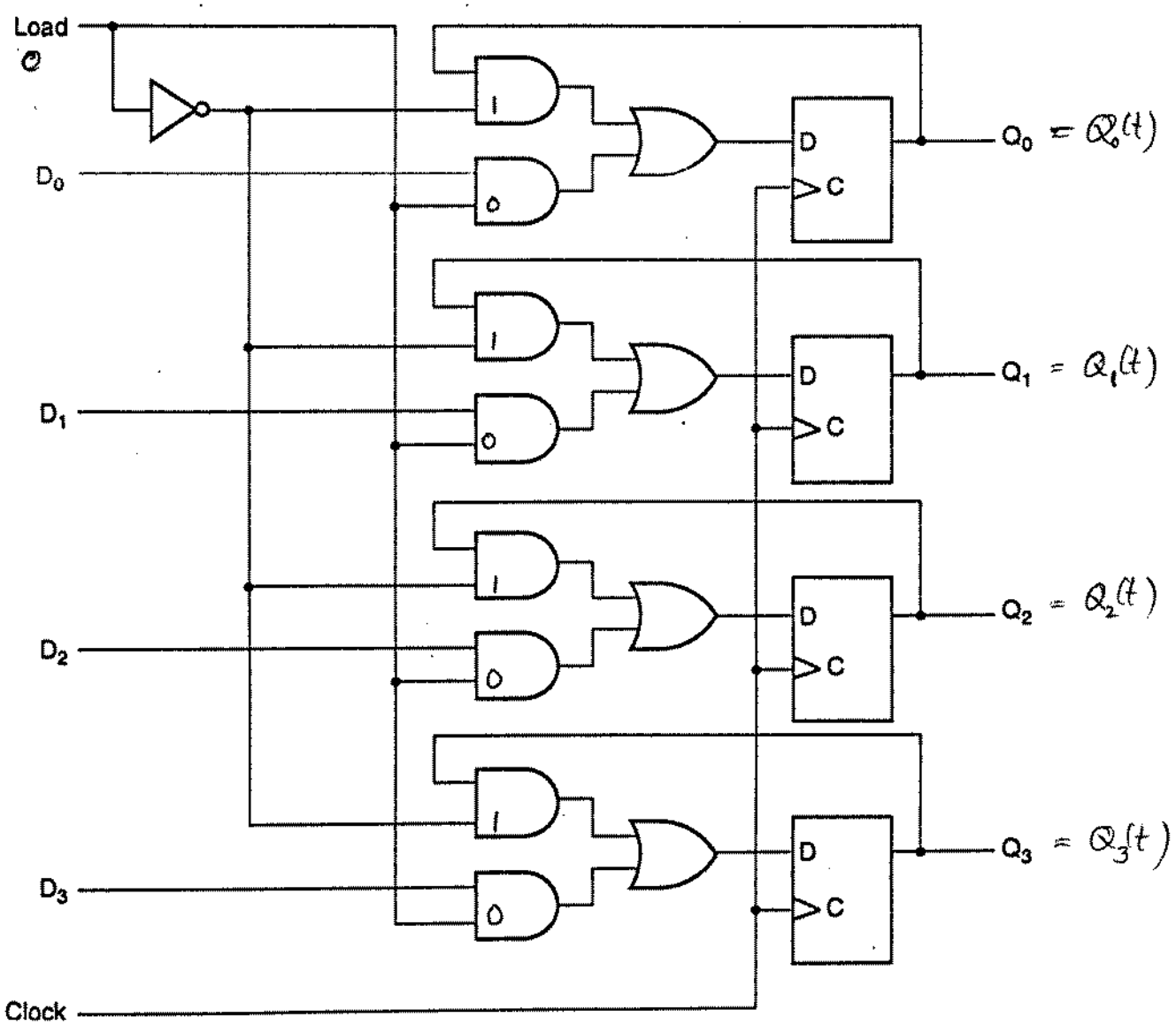
* **PARALLEL LOAD (TRANSFER IN PARALLEL MODE)**
TRANSFER OF NEW BINARY INFO INTO A REGISTER AS A WHOLE WORD
(# OF CLOCK PULSES NEEDED TO LOAD THE REGISTER = 1)

e.g., Let A and B be two n-bit registers

$A_n \quad A_2A_1$

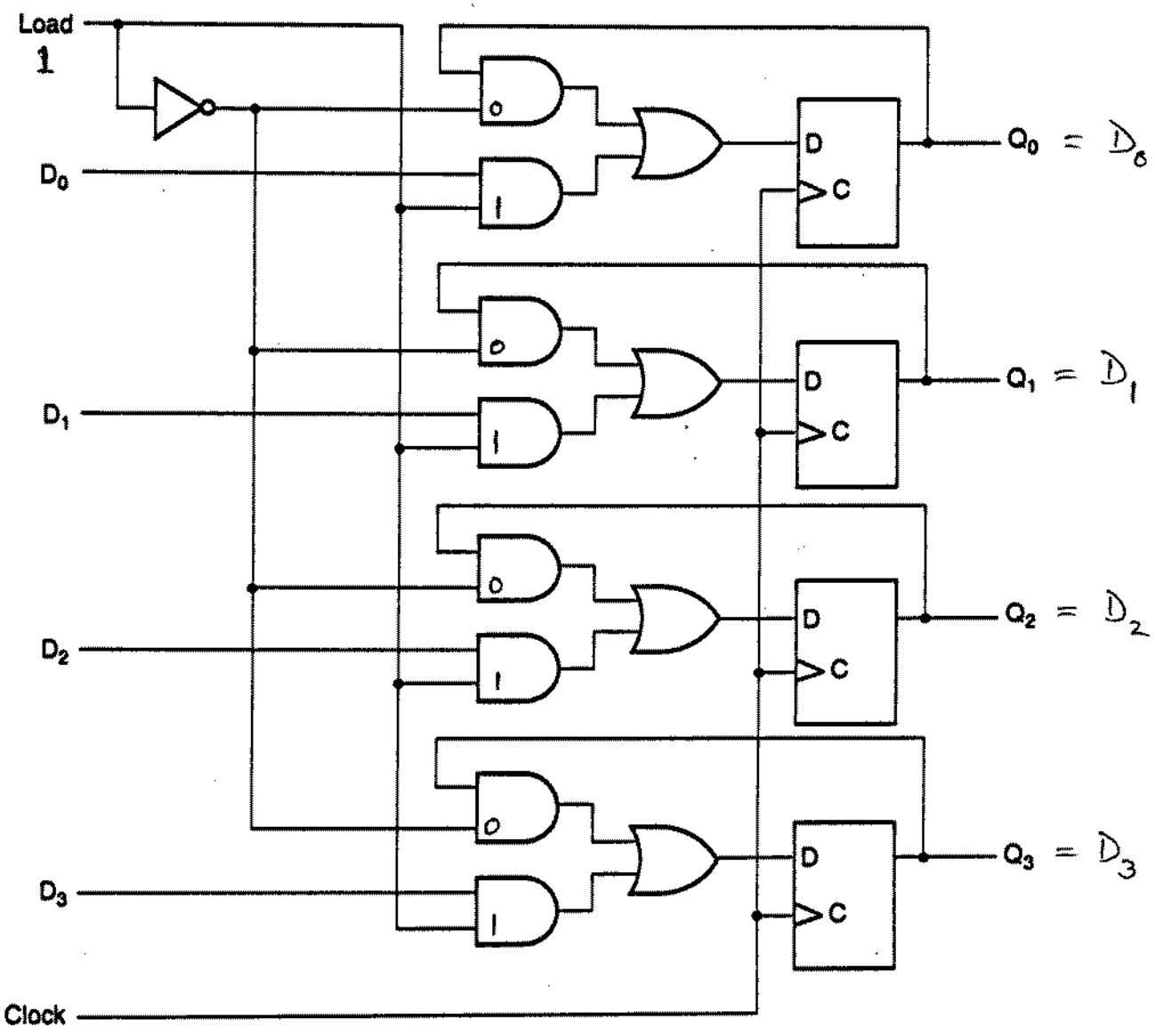
$B_n \quad B_2B_1$

e.g., 4-Bit Register with Parallel Load READ



e.g., 4-Bit Register with Parallel Load

After write, turn load to 0.



SHIFT REGISTER

A REGISTER CAPABLE OF SHIFTING ITS BINARY INFO TO ITS LEFT OR RIGHT

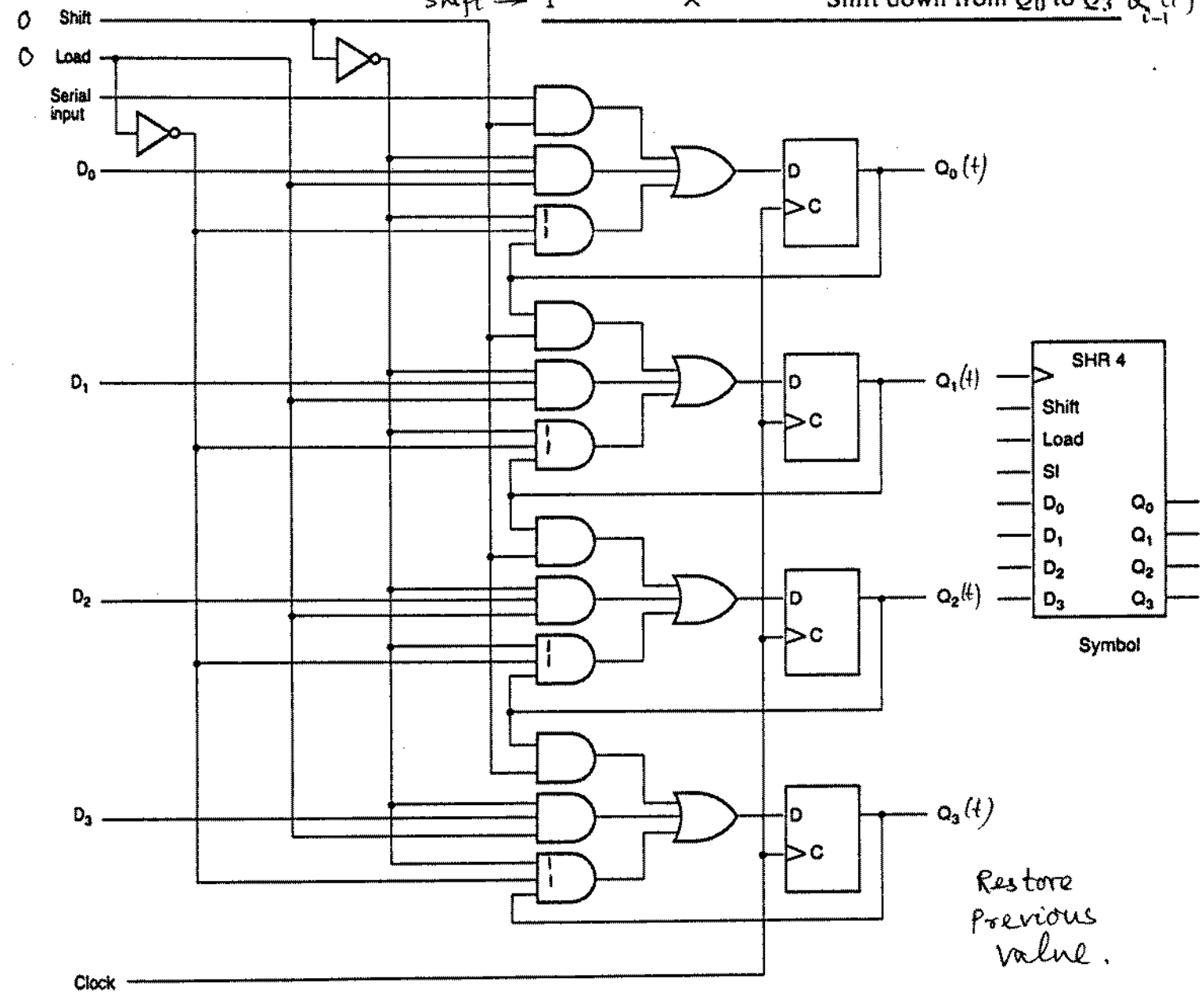
A REGISTER WHERE RS OR D FF'S ARE CONNECTED IN CASCADE

- UNIDIRECTIONAL SHIFT REGISTER
- BIDIRECTIONAL SHIFT REGISTER

If all the flip-flop outputs of a shift register are accessible, then information entered serially by shifting can be taken out in parallel from the outputs of all of the flip-flops. If a parallel load capability is also added to a shift register, then data entered in parallel can be taken out in serial fashion by shifting out the data in the register. Thus, a shift register with accessible flip-flop outputs and parallel load can be used for converting incoming parallel data to outgoing serial data and vice versa.

Shift Register with Parallel Load

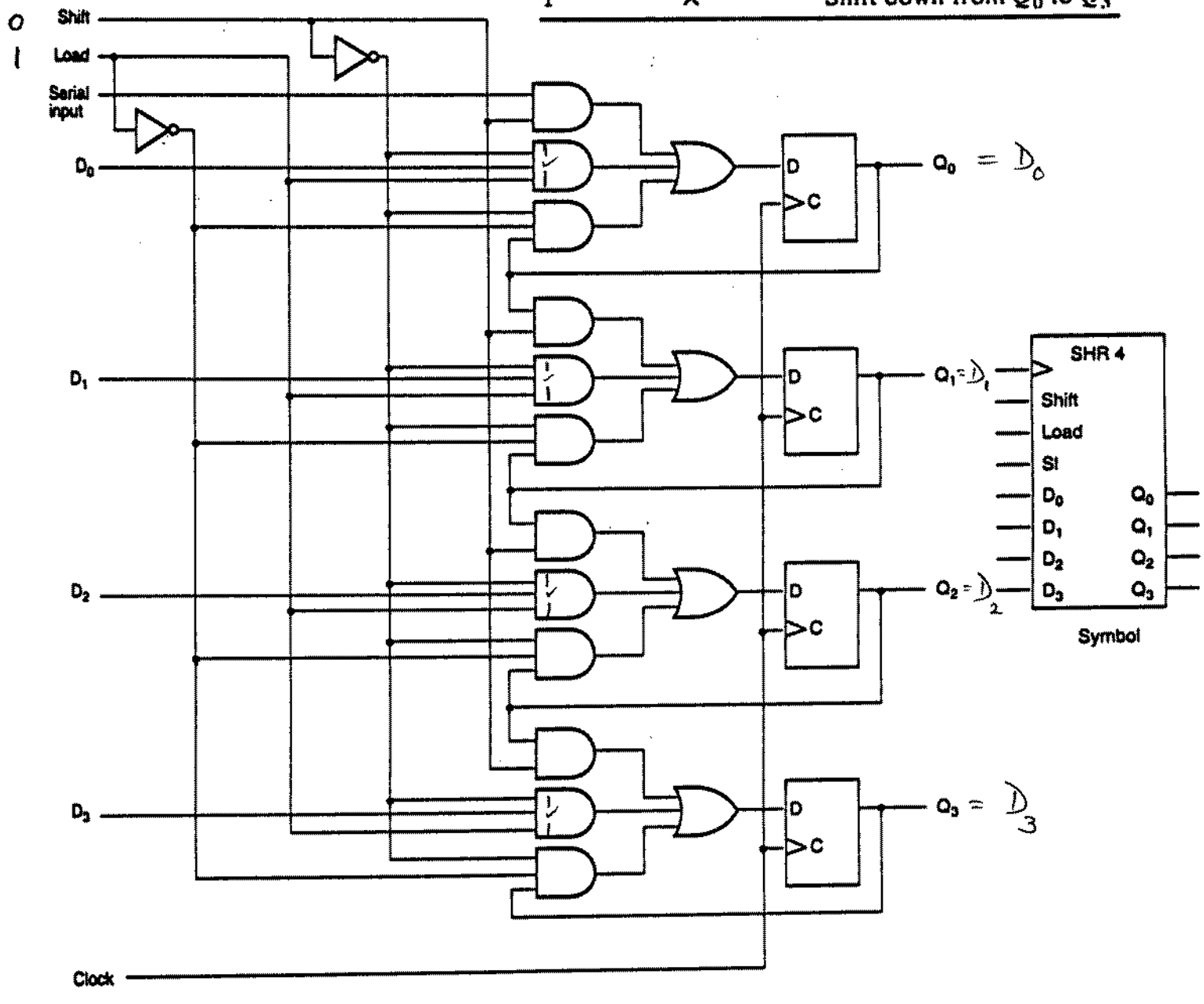
	Shift	Load	Operation	$Q_i(t+1)$
read →	0	0	No change	$Q_i(t)$
write →	0	1	Load parallel data	D_i
shift →	1	×	Shift down from Q_0 to Q_3	$Q_{i-1}(t)$



Shift Register with Parallel Load

Shift	Load	Operation
0	0	No change
→ 0	1	Load parallel data
1	×	Shift down from Q_0 to Q_3

Write



- Supply a value by Serial Input.

Shift Register with Parallel Load

Shift	Load	Operation
0	0	No change
0	1	Load parallel data
1	×	Shift down from Q_0 to Q_3