

A summary of the 680X0's instruction types (excluding floating-point instructions).

<i>Instruction type</i>	<i>Opcode</i>	<i>Description</i>
Data transfer	EXG	Exchange (swap) contents of two registers
	MOVE	Move (copy) data unchanged from source to destination
	SWAP	Swap left and right halves of register
Data processing	ABCD	Add decimal (BCD) numbers with carry (extend) flag
	ADD	Add binary (two's-complement) numbers
	AND	Bitwise logical AND
	AS _x	Arithmetic shift left ($x = L$) or right ($x = R$) with sign extension
	CLR	Clear operand by resetting all bits to 0
	DIV	Divide binary numbers
	EOR	Bitwise logical EXCLUSIVE OR
	EXT	Extend the sign bit of subword to fill register
	LS _x	Logical shift left ($x = L$) or right ($x = R$)
	MUL	Multiply binary numbers
	NBCD	Negate decimal number (subtract with carry from zero)
	NEG	Negate binary number (subtract from zero)
	NOT	Bitwise logical complement
	OR	Bitwise logical OR
	RO _x	Rotate left ($x = L$) or right ($x = R$)
	SBCD	Subtract decimal (BCD) numbers
	SUB	Subtract binary (two's-complement) numbers
Program control	Bcc	Branch relative to <i>PC</i> if specified condition <i>cc</i> is true
	BRA	Branch unconditionally, relative to <i>PC</i>
	BSR	Call (branch to) subroutine at address relative to <i>PC</i> ; save <i>PC</i> state (return address) in stack
	CMP	Compare two operand values and set flags based on result
	DBcc	Loop instruction: Test condition <i>cc</i> and perform no operation if condition is true; otherwise, decrement specified register and branch to specified address
	JMP	Branch unconditionally to specified address
	JSR	Call (jump to) subroutine at specified address; save <i>PC</i> state (return address) in stack
	NOP	No operation, but instruction execution continues
	RTS	Return from subroutine
	Scc	Set operand to 1s (0s) if condition <i>cc</i> is true (false)
	TST	Test an operand by comparing it to zero and setting flags

	<i>Transfer of Data</i>	<i>Effect</i>	<i>Restrictions</i>
	MOVE.size <s>,<d>	$\langle d \rangle \leftarrow \langle s \rangle$	$(\langle d \rangle \neq Ai)$
(Address)	MOVEA.size <s>,<d>	$\langle d \rangle \leftarrow \langle s \rangle$	$(\langle d \rangle = Ai) \text{ (size } \neq B)$
(Quick)	MOVEQ.size <s>,<d>	$\langle d \rangle \leftarrow \langle s \rangle$	$(\langle s \rangle = \text{Imm}) (\langle d \rangle \neq Ai) \text{ (size } \neq B W)$
	SWAP Di	$Di(31:16) \leftrightarrow Di(15:00)$	
	EXG Xi, Xj	$Xi(31:00) \leftrightarrow Xj(31:00)$	
	<i>Addition</i>		
	ADD.size <s>,<d>	$\langle d \rangle \leftarrow \langle d \rangle + \langle s \rangle$	$(\langle d \rangle \neq Ai) (\langle s \rangle \langle d \rangle = Di)$
(Address)	ADDA.size <s>,<d>	$\langle d \rangle \leftarrow \langle d \rangle + \langle s \rangle$	$(\langle d \rangle = Ai) \text{ (size } \neq B)$
(Immediate)	ADDI.size <s>,<d>	$\langle d \rangle \leftarrow \langle d \rangle + \langle s \rangle$	$(\langle s \rangle = \text{Imm}) (\langle d \rangle \neq Ai)$
	<i>Subtraction</i>	Same as ADD, but with keyword SUB	
	<i>Multiplication</i>	(restricted size: both operands are words)	
(Unsigned)	MULU <s>, Di	$Di(31:00) \leftarrow Di(15:00) * \langle s \rangle$	$(\langle s \rangle \neq Ai)$
(Signed)	MULS <s>, Di	$Di(31:00) \leftarrow Di(15:00) * \langle s \rangle$	$(\langle s \rangle \neq Ai)$
	<i>Division</i>	(restricted size: size of <s> = W)	
(Unsigned)	DIVU <s>, Di	$Di(31:00) \leftarrow Di(31:00) / \langle s \rangle$	$(\langle s \rangle \neq Ai)$
(Signed)	DIVS <s>, Di	$Di(31:00) \leftarrow Di(31:00) / \langle s \rangle$	$(\langle s \rangle \neq Ai)$
		Remainder = $Di(31:16) \&$ Quotient = $Di(15:00)$	
	<i>Other</i>		
	CLR.size <d>	$\langle d \rangle \leftarrow 0$	$(\langle d \rangle \neq Ai)$
	NEG.size <d>	$\langle d \rangle \leftarrow 2\text{'s C of } \langle d \rangle$	$(\langle d \rangle \neq Ai)$
	<i>Logical</i>		
	AND.size <s>,<d>	$\langle d \rangle \leftarrow \langle d \rangle \cap \langle s \rangle$	$(\langle d \rangle \neq Ai) (\langle s \rangle \langle d \rangle = Di)$
(Immediate)	ANDI.size <s>,<d>	$\langle d \rangle \leftarrow \langle d \rangle \cap \langle s \rangle$	$(\langle s \rangle = \text{Imm}) (\langle d \rangle \neq Ai)$
	OR.size <s>,<d>	$\langle d \rangle \leftarrow \langle d \rangle \cup \langle s \rangle$	$(\langle d \rangle \neq Ai) (\langle s \rangle \langle d \rangle = Di)$
(Immediate)	ORI.size <s>,<d>	$\langle d \rangle \leftarrow \langle d \rangle \cup \langle s \rangle$	$(\langle s \rangle = \text{Imm}) (\langle d \rangle \neq Ai)$
	EOR.size <s>,<d>	$\langle d \rangle \leftarrow \langle d \rangle \oplus \langle s \rangle$	$(\langle s \rangle = Di) (\langle d \rangle \neq Ai)$
(Immediate)	EORI.size <s>,<d>	$\langle d \rangle \leftarrow \langle d \rangle \oplus \langle s \rangle$	$(\langle s \rangle = \text{Imm}) (\langle d \rangle \neq Ai) \text{ (size } \neq W)$
	NOT.size <d>	$\langle d \rangle \leftarrow \langle d \rangle'$	$(\langle d \rangle \neq Ai)$

Transfer of Control

Bcc <relative address or label>

Branch to (relative address or label) if condition (cc) is true

A) Conditional Transfer

cc	Name	Flag Conditions
CC	Carry clear	$C = 0$
CS	Carry set	$C = 1$
EQ	Equal to (0)	$Z = 1$
GE	Greater than or equal to	$N \oplus V = 0$
GT	Greater than	$(N \oplus V) + Z = 0$
HI	Higher than	$C + Z = 0$
LE	Less than or equal to	$(N \oplus V) + Z = 1$
LS	Less ^{Lower} than or the same as	$C + Z = 1$
LT	Less than	$N \oplus V = 1$
MI	Minus, or negative	$N = 1$
NE	Not equal to (0)	$Z = 0$
PL	Plus, or positive	$N = 0$
VC	No overflow	$V = 0$
VS	Result is too large	$V = 1$

B) Unconditional Transfer

JMP <relative address or label>

BRA <relative address or label>

Branch to (relative address or label) unconditionally

	<u>Compare</u>	<u>Effect</u>	<u>Restriction</u>
	CMP.size <s>, <d>	$? = \langle d \rangle - \langle s \rangle$	$\langle d \rangle = D_i$
(Address)	CMPA.size <s>, <d>	$? = \langle d \rangle - \langle s \rangle$	$\langle d \rangle = A_i$ (size $\neq B$)
(Immediate)	CMPI.size <s>, <d>	$? = \langle d \rangle - \langle s \rangle$	$\langle s \rangle = \text{Imm}$ ($\langle d \rangle \neq A_i$)
(Memory)	CMPM.size <s>, <d>	$? = \langle d \rangle - \langle s \rangle$	(Both $\langle s \rangle$ and $\langle d \rangle = (A_i) +$)

Class	Left shift	Right shift
ASL, arithmetic shift left ASR, arithmetic shift right		
LSL, logical shift left LSR, logical shift right		
ROL, rotate left ROR, rotate right Note X bit not affected		
ROXL, rotate left through extend ROXR, rotate right through extend		

Arithmetic shifts update *all* bits of the CCR. The N and Z bits are set or cleared as we would expect. The V bit is set if the most significant bit of the operand is changed at any time during the shift operation. The C and X bits are set according to the last bit shifted out of the operand. However, if the shift count is zero, C is cleared and X is unaffected. Logical shifts and rotates clear the V bit.

Assembly Language Form of Shift Operations

All eight shift instructions are expressed in one of three ways. These are illustrated by the ASL (arithmetic shift left) instruction.

Mode 1.	ASL Dx,Dy	Shift Dy by Dx bits
Mode 2.	ASL #<data>,Dy	Shift Dy by #data bits
Mode 3.	ASL <ea>	Shift the contents of ea by one place

A shift instruction can be applied to a byte, word, or longword operand, with the exception of mode 3 shifts, which act only on words.

In mode 1, the "source" operand, Dx, specifies how many places the destination operand, Dy, needs to be shifted. Dy may be shifted by 1 to 32 bits. In mode 2, the literal, #<data>, specifies how many places Dy needs to be shifted; this must be in the range 1 to 8. In mode 3, the memory location specified by the effective address, <ea>, is shifted one place. Many microprocessors permit only the *static* shifts of modes 2 and 3. The 68000 permits *dynamic* shifts (i.e., mode 1) because the number of bits to be shifted is computed at run-time.

ASSEMBLER DIRECTIVES

(Allocate storage, Define constants, Link identifiers to values, control assembling)

DS

DC

EQU

A line starting at column 1 with an * is a comment.

Any other line is composed of three parts:

- Label (starts at column 1 with a letter and consists of at most 8 characters)
- instruction or assembler directive
- Comment

(1st and 3rd parts are optional. If label is not used then column 1 is empty)

TTL (gives the title of the program)

identifier EQU value (links an identifier to a value)

ORG \$HHHHHH (Origin of data)

identifier DS.size length (reserves memory space for variables)

identifier DC.size value (defines constants)

ORG \$HHHHHH (Origin of program)

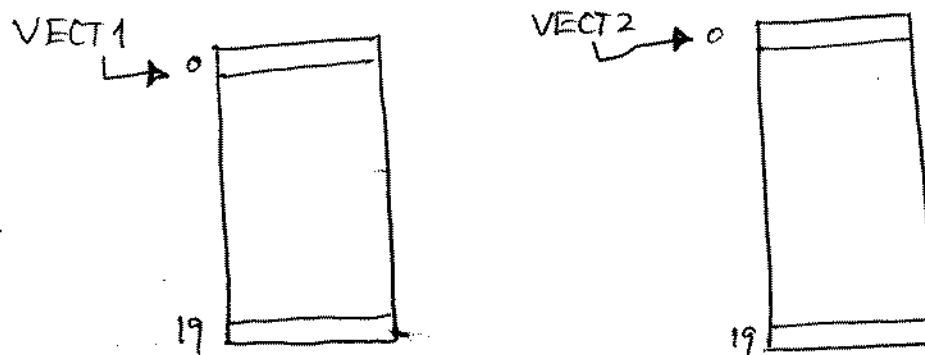
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INSTRUCTIONS ARE PLACED HERE

.....

END (indicates the end of the program)

- a) Given two vectors of 20 one-byte numbers each, located at addresses VECT1 and VECT2.



Add these vectors and put the resulting vector at address VECT2.

AddVect:

```
CLR.L    D0
MOVEA.L  VECT1, A0
MOVEA.L  VECT2, A1
```

$D_0 \leftarrow 0$
 $A_0 \leftarrow \text{VECT1}$
 $A_1 \leftarrow \text{VECT2}$

Loop:

```
MOVE.B   (A0)+, D1
```

$D_1 \leftarrow M[A_0]; A_0 \leftarrow A_0 + 1$

```
ADD.B    D1, (A1)+
```

$M[A_1] \leftarrow M[A_1] + D_1; A_1 \leftarrow A_1 + 1$

```
ADDI.B   #$1, D0
```

$D_0 \leftarrow D_0 + 1$

```
CMPI.B   #20, D0
```

$D_0 - 20$ (#14) ?

```
BNE      Loop
```

if \neq , branch to Loop.

Done:

Note that

```
ADD.B    D1, (A1)+
can be replaced by
ADD.B    D1, (A1)
ADDA.L   #1, A1
```

- b) Given a vector of 10 one-byte numbers, located at address NUMBERS. Find the sum (address SUM) and the average (address AVERAGE) of these numbers.

Stats:

```
CLR.L    D0
MOVE.B   #10, D1
CLR.L    D2
MOVEA.L  NUMBERS, A0
```

~~D0 ← 0~~ $D_0 \leftarrow 0$
 $D_1 \leftarrow 10$
 $D_2 \leftarrow 0$
 $A_0 \leftarrow \text{NUMBERS}$

Loop:

```
MOVE.B   (A0)+, D2
```

$D_2 \leftarrow M[A_0]; A_0 \leftarrow A_0 + 1$

```
ADD.L    D2, D0
```

$D_0 \leftarrow D_0 + D_2$

```
SUBI.B   #1, D1
```

$D_1 \leftarrow D_1 - 1$

```
BNE      Loop
```

if ($D_1 \neq 0$) branch to Loop

```
MOVE.W   D0, SUM
```

$M[\text{SUM}] \leftarrow D_0$

```
DIVU     #10, D0
```

$D_0.W \leftarrow D_0 / 10$

```
MOVE.B   D0, AVERAGE
```

$M[\text{AVERAGE}] \leftarrow D_0$

Done: