Short introduction to VHDL for Max+plus II

Daniel Amyot
damyot@site.uottawa.ca

VHDL

- **V**ery High Speed Integrated Circuit (VHSIC) **H**ardware **D**escription **L**anguage
- IEEE Std. 1076 (-1998, -1993, …)
  - Description and analysis of logic circuits
- IEEE Std. 1164
  - Multivalued logic
    - 9 are defined (0,1, X, high impedance, …)
  - Used in VHDL for the logic variables

Why VHDL?

- Description (systems and components)
- Simulation and analysis
- Synthesis of circuits
- Implementation

- We will concentrate one the first 2 aspects.

Temporal and Functional Analysis

- Temporal Analysis
  - Takes into account delays (see assignment 1)
- Functional Analysis
  - Logical aspects only
  - No delays

Example: adder (assignment 1)

```
-- Realisation of S(X,Y) = XY' + X'Y  and  C(X,Y) = XY

LIBRARY ieee;
USE ieee.std_logic_1164.all;

-- Inout/output function variables
ENTITY adder IS
   PORT(X, Y     : IN   STD_LOGIC;  -- Inputs
        S, C     : OUT  STD_LOGIC); -- Outputs
END adder ;

-- Outputs as fonction of inputs
ARCHITECTURE logic OF adder IS
BEGIN
  S <= (X AND (NOT Y)) OR ((NOT X) AND Y);
  C <= X AND Y;
END logic;
```

Operators and constants

- Supported core operators
  - NOT
  - AND
  - OR
  - XOR
  - XNOR
  - NAND
  - NOR
- Constants
  - '1'
  - '0'

Temporal Analysis (with delays)

Generation of truth tables

Truth Table (placed in file .tbl) - Temporal Analysis

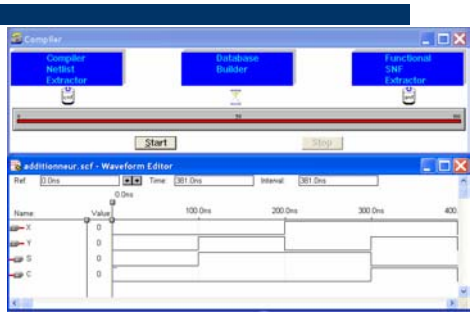
```
%       X Y   S C %

   0.0> 0 0 = 0 0
 100.0> 0 1 = 0 0
 110.4> 0 1 = 1 0
 200.0> 1 0 = 1 0
 209.9> 1 0 = 0 1
 210.4> 1 0 = 1 0
 300.0> 1 1 = 1 0
 310.4> 1 1 = 0 1
 400.0> 0 0 = 0 1
```

- Note
  - Change happens after the delay, but not when X and Y changes…
  - Similar combinations of X and Y leads to different outputs!
  - Some tables generated are difficult to understand
- Need to preserve the time interval necessary for verifying all combinations
- Put X and Y in order!

Looking into functional analysis…

Temporal Analysis (without delays)



Truth Table (placed in file .tbl) - Functional Analysis

```
%       X Y   S C %

   0.0> 0 0 = 0 0
 100.0> 0 1 = 1 0
 200.0> 1 0 = 1 0
 300.0> 1 1 = 0 1
 400.0> 0 0 = 0 0
 500.0> 0 1 = 1 0
 600.0> 1 0 = 1 0
 700.0> 1 1 = 0 1
 800.0> 0 0 = 0 0
 900.0> 0 1 = 1 0
1000.0> X X = X X
```

- Only the combinations from 0.0 to 300.0 are necessary
  - 2 variables, 100 ns are necessary
  - For assignment # 2?