Assignment # 3 - CSI 2111

Due Friday **November 11, 2005** by 16:00,
in box marked CSI2111 (#31) in 1st floor of SITE building.
This assignment should be done in teams of two people.

Clearly identify all the steps for each question.

Q1. Realize, using a suitable PLA, the following functions : [10 marks]

$f_1(x,y,z) = \Sigma m(0,1,5,7)$
$f_2(x,y,z) = \Sigma m(2,5,6)$
$f_3(x,y,z) = \Sigma m(1,4,5,7)$
$f_4(x,y,z) = \Sigma m(0,3,6)$

Minimize the number of product terms and show all connections.

Q2. Design a 4-bits arithmetic unit with two input selection lines (S_1 and S_0) which generates the following arithmetic operations: [10 marks]

$S_1 S_o$	$\mathbf{C_{in} = 0}$	$\mathbf{C_{in} = 1}$
00	$G = B'$ (complement)	$G = B' + 1$ (negation 2CF)
01	$G = A - 1$ (decrement)	$G = A$ (transfer)
10	$G = bbbb$ (invalid operation)	$G = A + B' + 1$ (subtraction)
11	$G = A + B$ (addition)	$G = bbbb$ (invalid operation)

Suppose $A = A_3A_2A_1A_0$, $B = B_3B_2B_1B_0$, and $G = G_3G_2G_1G_0$. $G = bbbb$ is an unspecified combination of bits which cannot be used as valid result. Use elementary adders and multiplexers in your realization. Add also the logical circuits necessary for the calculation of the bits of state N, Z, V, C, and W (bit indicating *invalid operation* when W=true)

Q3. Consider the following sequential circuit: [10 marks]

$J_A = [(AX')'(A'X)']'$
$J_B = (B'+ X')'$
$K_A = AX'$
$K_B = (A'+ X')'$
$Z = (A + B)'$

a) Construct the transition table for this circuit
b) Construct the transition diagram for this circuit
c) Determine the state equations of the circuit
d) What is the output sequence when one applies the input sequence 01100 to X (the circuit is initially with state AB=00)

Q4. The following transition table describes a sequential circuit: [10 marks]

Present State	Next State x=0	Next State x=1	Output x=0	Output x=1
A B	A B	A B	z	z
0 0	0 0	0 1	1	0
0 1	0 1	1 0	0	1
1 0	1 0	1 1	1	0
1 1	1 1	1 1	0	1

a) Determine the state equations and output of this circuit.
b) Realize this using D flip-flops.
c) Realize this using RS flip-flops.

Q5. (a) Implement in VHDL, a sequential circuit that takes three signals (Load, ShiftLeft, ShiftRight) and a 8-bit InputValue. Additionally, the circuit has an input Clock signal. The circuit output is a 8-bit OutputValue. The circuit operates on the rising edge of the clock, according to the following rules: [15 marks]

- If Load == 1, then it remembers the 8-bit InputValue. The remembered value is output as a 8-bit value OutputValue.
- ELSE If ShiftLeft == 1, then it updates the remembered value to be its previous value shifted to the left by one bit. The remembered value is output as a 8-bit value OutputValue.
- ELSE If ShiftRight == 1, then it updates the remembered value to be its previous value shifted to the right by one bit. The remembered value is output as a 8-bit value OutputValue.
- ELSE OutputValue is unchanged.

(b) Simulate the circuit that you implemented and test it for the following inputs (in the order as they appear): [5 marks]

1. When LOAD = 1, ShiftLeft = 0, ShiftRight = 0, InputValue = 01100101
2. When LOAD = 0, ShiftLeft = 1, ShiftRight = 0, InputValue = 00000000
3. When LOAD = 0, ShiftLeft = 0, ShiftRight = 1, InputValue = 11111111
4. When LOAD = 1, ShiftLeft = 0, ShiftRight = 1, InputValue = 11110000
5. When LOAD = 0, ShiftLeft = 0, ShiftRight = 1, InputValue = 00000001

Submit the timing diagram showing all the above test cases. (Note that for each test case, you need to show what happens on a rising edge of the Clock.)