Assignment # 2 - CSI 2111

Due Tuesday **October 18, 2005** by 16:00,
in box marked CSI2111 (#31) in 1st floor of SITE building.
This assignment should be done in teams of two people.

<u>Clearly identify all the steps for each question.</u>

Q1. We need to design a full subtractor which computes $a - b - c$, where c is the borrow from the next less significant digit that produces a difference, d, and a borrow from the next more significant bit, p.

a) Give the truth table for the full subtractor. (5)

b) Implement the circuit using only NAND gates and inverters . (5)

Q2. a) Implement, with a decoder and external OR gates, the combinational circuit specified by the following three Boolean functions: (5)

$f_1(A, B, C) = \Sigma m(0,3,4)$
$f_2(A, B, C) = \Sigma m(1,2,7)$
$f_3(A, B, C) = \Pi M(0,1,2,4)$

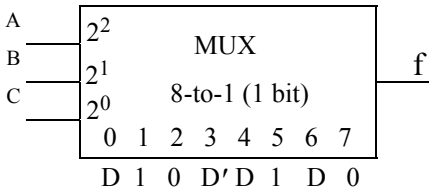
b) Design a 4-to-16 line decoder with *Enable* input using five 2-to-4 line decoders with *Enable* inputs. (5)

Q3. a) Implement the following Boolean function with an 8-to-1 line multiplexer and a single inverter with variable B as an input. (5)

$$f(A, B, C, D) = \Sigma m(2, 4, 6, 9, 10, 11, 15)$$

b) Give the canonical sum of product expression for the function which is implemented using the following circuit.

(5)



Q4. a) Given a 256 x 8 ROM chip with *Enable* input, show the external connections necessary to construct a 2K x 8 ROM with eight chips and a decoder. (5)

b) Specify the size of a ROM (number of words and number of bits per word) necessary to implement a binary multiplier that multiplies two 8-bit numbers. (5)

Q5. Consider the function ***f*** (w, x, y, z) = Σm (1, 3, 7, 11, 13, 14, 15).

a) Implement *f* in VHDL, using AND, OR, NOT gates. Call it *circuit5a*. (5)

b) Implement *f* in VHDL, but use **only** NAND gates (no NOT gates!). Call it *circuit5b*. (5)

b) Implement *f* again in VHDL, but use **only** NOR gates this time. Call it *circuit5c*. (5)

b) Compare the simulation results of the three implementations in VHDL for all combinations of the inputs *w, x, y, z*. Please include the timing diagram (0 ns to 1600 ns) and the truth tables for 1a), 1b), and 1c) and explain the differences, if any. (5)

For this question, use Max+plus II in the *Functional SNF Extractor* mode. This mode eliminates the signal transmission delays, which makes checking the equivalence between two functions easier.