# *Assignment #1 - CSI 2111*

Due Friday, **September 30,** 2005 before 16:00,
in box marked CSI2111 (**#31**) 1st floor of SITE building.

**This assignment could be done in teams of two people.**

**<u>Clearly identify all steps for each question.</u>**

The number of points of each question is indicated between brackets, for a total of 70 points.

Q1. Consider binary words of length N = 8 bits, representing signed numbers.
a) Find the 2's CF representation of the numbers: $(+63)_{10}$, $(-63)_{10}$, $(+115)_{10}$, $(-115)_{10}$. (4)
b) Using 2's CF representation, calculate: $(+115)_{10} + (-63)_{10}$ (2)
c) Using 2's CF representation, calculate: $(-115)_{10} - (-63)_{10}$ (2)

Q2. Consider signed numbers of length N = 6 bits in 2's CF representation.
Using Booth algorithm, calculate: $(-30)_{10} * (-17)_{10}$. (8)

Q3. a) Identify the decimal number in floating point represented in IEEE 754 form by: (4)
( 1 10001011 11101000000000000000000 )$_{IEEE754}$ = ( ? )$_{10}$
b) Represent the decimal number $(-221.390625)_{10}$ in IEEE 754 form. (4)

Q4. By indicating the axioms and theorems used in each step, where applicable:
a) Complement the Boolean function: $\boldsymbol{f}$ (w, x, y, z) = (w + x + y)(w' + xz) + y'z' (4)
b) Prove **algebraically** that: $B + C'D = AB + BC'D' + A'BC + C'D$ (6)

Q5. Let $\boldsymbol{f}$ (w, x, y, z) = ΠM (0, 2, 4, 5, 6, 8, 12) :
a) Determine the <u>minimal</u> SOP form of $\boldsymbol{f}$. (4)
b) Determine the <u>minimal</u> POS form of $\boldsymbol{f}$. (4)

Q6. Let $\boldsymbol{f}$ (w, x, y, z) = Σm (1, 3, 4, 6, 8, 11) X (0, 5, 14) :
a) Determine the <u>minimal</u> SOP form of $\boldsymbol{f}$. (4)
b) Determine the <u>minimal</u> POS form of $\boldsymbol{f}$. (4)

Q7. Using Max+plus II (without VHDL):
a) Give graphical representation (using the *Graphic Editor*) for the following two functions: (10)
F1$(X,Y,Z) = (XY + Z')(X + Y'Z')$ and
F2$(X,Y,Z) = ((XY + Z')(X + Y'Z'))'$
Use only the components: and2, or2, not, input, output

b) Simulate your circuit using all the combinations of 0's and 1's for X, Y and Z. (10)
Include in your assignment the timing diagram resulting with, (in this order) the input signals *X, Y* and *Z* and the outputs *F1* and *F2*. You can use the total time interval of 800ns (100ns clock period).

**Note**: You may simply include a screen capture (using cut/paste) of your circuit diagram and the resulting timing diagram (signals). They must however be readable.