

Instrumentation Applications of Multibit Random-Data Representation

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Abstract—Extrapolating the von Neuman’s random-pulse machine concept, the paper discusses the multibit random-data representation and shows how it can be used for the modular design of robust instrumentation for real-time statistical parameter estimation and especially of hardware neural networks.

I. INTRODUCTION

HYBRID instrumentation and signal processing architectures using pulse stream techniques are known to offer the best of both digital and analog technologies. Some of these techniques use pulse amplitude, width, density, or frequency encoding methods for signal representation, while other techniques use probabilities of streams of random pulses.

The latter approach was first presented by von Neumann in 1956 [1]. A number of similar stochastic data-processing concepts were reported in the 1960s: *noise computer*, [2], *random-pulse machine*, [3], and *stochastic computing* [4]. In the case of the random-pulse machines, the analog variables are represented by the mean rate of random-pulse streams. Such a representation can be viewed as the probability modulation of a random-pulse carrier by a deterministic analog variable. Simple digital gates can be used to perform 1-bit arithmetic and logic operations. This concept presents a good tradeoff between electronic circuit complexity and computational accuracy. The relatively low circuit complexity was exploited during the 1960s for the construction of cost-effective instrumentation [5] and [6]. More recently, there is a renewed interest in random-pulse data systems as their high packing density makes them quite suitable for the VLSI implementation of parallel signal processors and neural networks (NNs) [7]–[10].

In parallel with the random-pulse data processing research, there has been an ongoing interest, from an instrumentation and measurement perspective, in the study of the dithered quantization and its applications to the analog-to-digital conversion [11]–[23].

Random-pulse data representations are produced by a 1-bit dither quantization, as illustrated in Fig. 1. A dither signal R uniformly distributed between $+FS$ and $-FS$ is added to the analog input V before quantization. The resulting analog random signal

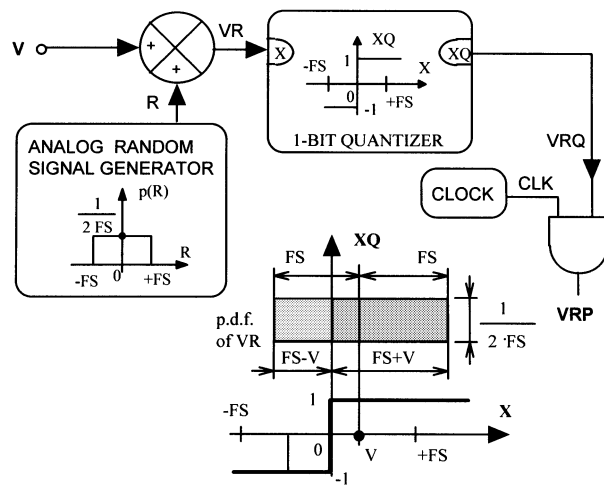


Fig. 1. 1-bit analog/random-pulse conversion.

VR is then 1-bit quantified to produce a random sequence of pulses VRP which will have the binary value $+1$ if $VR \geq 0$ -1 if $VR < 0$.

The deterministic component of the random-pulse sequence can be calculated as a statistical estimation from the quantization diagram given in Fig. 1

$$\begin{aligned}
 E[VRP] &= (+1) \cdot p[VR \geq 0] + (-1) \cdot p[VR < 0] \\
 &= p[VRP] - p(VRP') \\
 &= \frac{FS + V}{2 \cdot FS} - \frac{FS - V}{2 \cdot FS} = \frac{V}{FS}
 \end{aligned} \tag{1}$$

which finally gives the deterministic analog value V associated with the binary VRP sequence

$$V = [p(VRP) - p(VRP')] \cdot FS \tag{2}$$

where the apostrophe ($'$) denotes a logical inversion.

As variables are represented by statistical averages of random pulse streams, the resulting data processing system has a better tolerance to noise than classical deterministic systems. The digital technology used to implement random-pulse machines offers a number of advantages over the analog technology: modular and flexible design, higher internal noise immunity, and simpler I/O interfaces. An important drawback is the relatively long time needed to get an acceptable accuracy for these statistical averages. However, the effects of this drawback can be mitigated by using data produced by multibit dithered quantization [6] and [13].

This paper proposes a generalization of the random-pulse machine concept, namely the multibit random-data machine,

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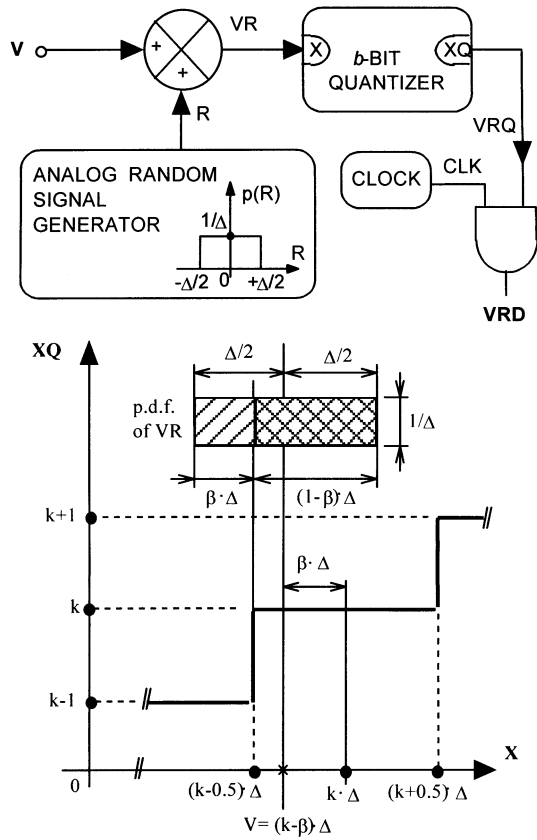


Fig. 2. Multibit analog/random-data conversion.

and shows how it can be used for a modular design of robust instrumentation for statistical signal processing and especially for hardware NNs. Variables are represented by probabilities of streams of random multibit data. The advantage of using multibit data instead of pulses (which are 1-bit data) is a considerable reduction in the time needed to get an acceptable accuracy for the statistical averages of the data streams carrying the information. As in the case of the random-pulse machine, the arithmetic operations are performed by relatively simple logic circuits. The resulting hardware implementation of specific signal processing or NN functions has inherently a higher processing speed than any software implementation.

II. MULTIBIT RANDOM DATA REPRESENTATION

The multibit random-data representation is produced by multibit analog/random-data conversion, or multibit dithered quantization (Fig. 2).

The analog input V , supposed to have a relatively low variation rate, is added to an analog random dither signal R uniformly distributed between $+\Delta/2$ and $-\Delta/2$, which shall fulfill the following statistical requirements [6] and [13]: i) zero mean, ii) independent of the input V , and iii) characteristic function having periodic zeros. The resulting analog signal VR is quantified with a b -bit resolution and then sampled by a clock CLK to produce the random sequence VRD of b -bit data having amplitudes restricted to two sequential quantized values $k-1$ and k .

The ideal estimation over an infinite number of samples of the random-data sequence VRD can be calculated from the quantization characteristic given in Fig. 2

$$\begin{aligned} E[VRD] &= (k-1) \bullet p[(k-1.5)\Delta \leq VR < (k-0.5)\Delta] \\ &\quad + k \bullet p[(k-0.5)\Delta \leq VR < (k+0.5)\Delta] \\ &= (k-1) \bullet \beta + k \bullet (1-\beta) = k - \beta. \end{aligned} \quad (3)$$

How good an estimation of V is actually obtained depends on the initial quantization resolution Δ , the finite number of samples that are averaged, and on the statistical properties of the dither signal R .

Random-pulse representation can be considered as a particular case of the multibit random-data representation, when $b = 1$.

A. Random-Data/Analog Conversion

The deterministic component V of the random-data sequence could be estimated as the average V_N^* over the finite set of the most recent N random data $\{VRD_i/i = 1, 2, \dots, N\}$. The accuracy of such estimation could be improved by increasing the size N of the set of random data that is averaged. On the other hand, when the random-data sequence represents a time-varying input signal, then the random-data/analog converter must have the ability to track the signal continuously, or else the higher frequency components of the input signal will be lost. This requires the averaging of smaller sets of random data.

A *moving average* algorithm eliminates the need to continuously recalculate the sum of the most recent N data and then divide it by N . This technique [24]–[25] is described by the equation

$$V_N^* = \frac{1}{N} \sum_{i=1}^N VRD_i = \frac{1}{N} \left(\sum_{i=1}^{N-1} VRD_i + VRD_N \right) \quad (4)$$

which yields

$$V_N^* = V_{N-1}^* + \frac{VRD_N - VRD_0}{N}. \quad (5)$$

The last equation shows that when a new VRD_N sample is taken into consideration, the new value of the average can be calculated by adding the new sample and deleting the oldest sample VRD_0 . While the straightforward averaging algorithm requires the addition of N samples, this iterative algorithm requires only an addition and a subtraction. The price for this simplification and acceleration of the arithmetic operations is the need to store and continuously update the whole sequence of the most recent N samples.

Figs. 3 and 4 show the normalized mean absolute error and, respectively, the normalized mean square error for 1-bit and 2-bit quantization functions of the moving average window size N . These results were obtained over a total number of 256 random-data samples.

III. ARITHMETIC OPERATIONS WITH MULTIBIT RANDOM-DATA REPRESENTATIONS

One of the most attractive features of the random-pulse data representation is that simple logical operations with individual

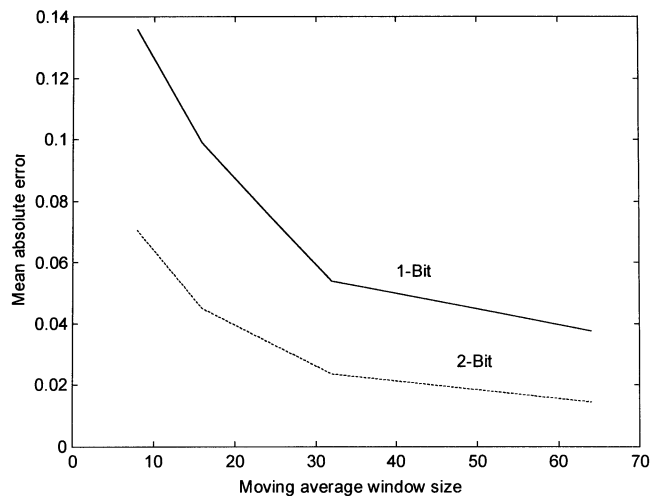


Fig. 3. Normalized mean absolute error function of the moving average window size.

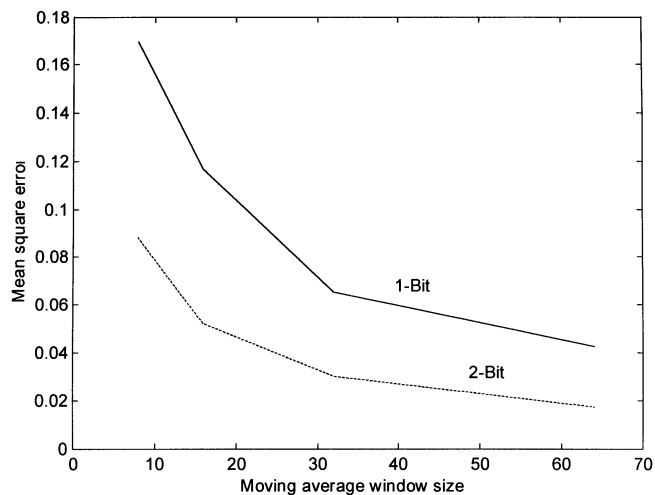


Fig. 4. Normalized mean square error function of the moving average window size.

pulses allow arithmetic operations with the analog variable represented by their respective random-pulse sequences to be carried out [3] and [4]. This feature is still present in the case of low bit-number random-data representations, which also yield a substantial increase in the overall resolution when compared with the random-pulse representation.

A. Addition

The arithmetic addition of m b -bit random-data samples X_1, X_2, \dots, X_m can be carried out as shown in Fig. 5 by a time multiplexing controlled by random signals $S_i (i = 1, 2, \dots, m)$.

The random scanning acts as a *stochastic isolator* [4], which removes unwanted correlations between sequences with similar patterns. The random scanning signals S_i are uniformly distributed having the same probability: $p(S_i) = 1/m$. Because of this scanning, the multiplexed samples are statistically independent. The analog meaning of the output sequence is $Z = (X_1 + \dots + X_m)/m$.

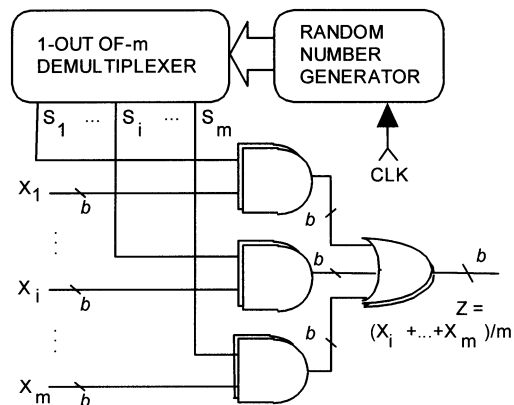


Fig. 5. Stochastic adder for random-data.

TABLE I
TRUTH TABLE FOR THE MULTIPLICATION
OF TWO 2-BIT RANDOM-DATA OPERANDS

		Y		
		0	1	-1
X	0	00	01	10
	1	00	10	-10
	-1	00	-10	10

B. Multiplication

We will consider further the case of 2-bit unbiased and signed random data produced by a dithered 2-bit quantizer. The truth table for the multiplication of two 2-bit random-data samples represented in 1s complement form $Z = X * Y$ is given in Table I.

From this table, we obtain the logic equations for the most-significant bit Z_{MSB} and the least-significant bit Z_{LSB} of a 2-bit sample of the product Z

$$Z_{MSB} = X_{LSB} \cdot Y_{MSB} + X_{MSB} \cdot Y_{LSB} \quad (6)$$

$$Z_{LSB} = X_{MSB} \cdot Y_{MSB} + X_{LSB} \cdot Y_{LSB} \quad (7)$$

where X_{MSB} and Y_{MSB} are the most-significant bits, and X_{LSB} and Y_{LSB} are the least-significant bits of the X and Y random-data samples. Fig. 6 shows the resulting logic circuit for this 2-bit multiplier.

Fig. 7 shows as an example the result, labeled *product*, of the 2-bit random data multiplication of two variables, labeled *weight* and *input*. Because of the relatively small window size, $N = 32$, used in this case by the moving-average algorithm (5), the recovered result is rather noisy. Its shape would have been smoother for a larger window size.

IV. MEASUREMENT INSTRUMENTATION USING MULTIBIT RANDOM-DATA REPRESENTATION

An analog/digital converter consists of an analog/random-data converter followed by a random-data/dig-

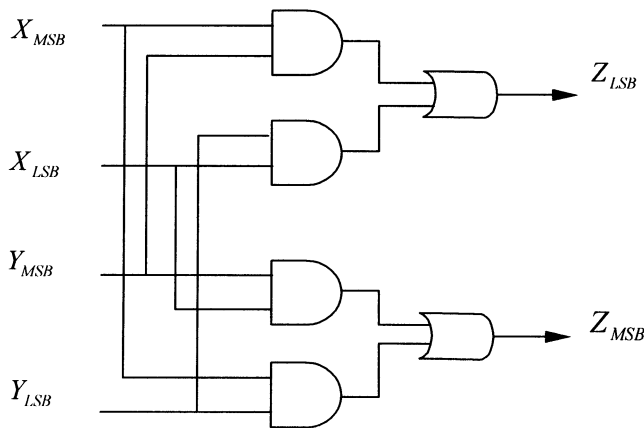


Fig. 6. 2-bit random-data multiplier.

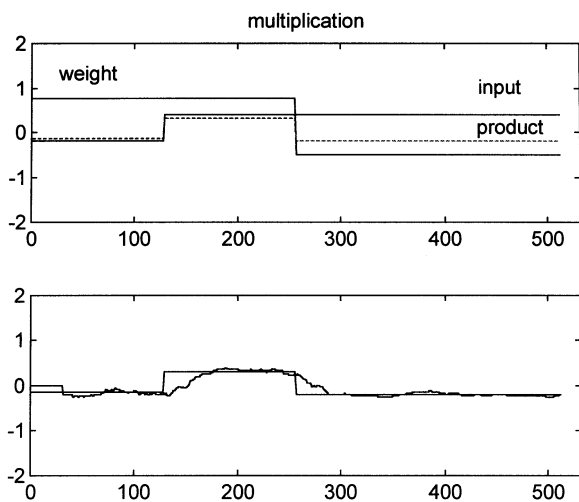


Fig. 7. Example of 2-bit random-data multiplication.

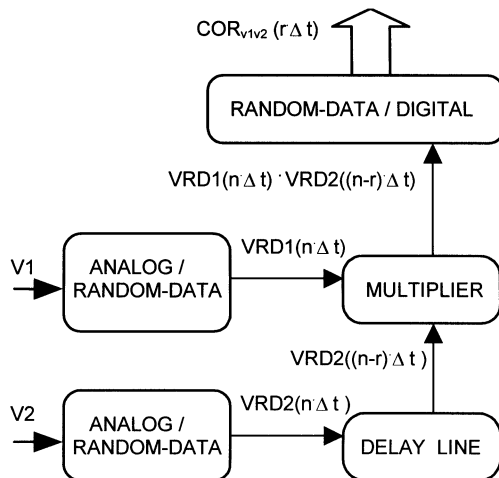


Fig. 8. Modular architecture of a serial-type correlator using multibit random-data representation.

ital converter. A final digital display is added if the analog/digital converter is to be used as a digital voltmeter.

Fig. 8 shows the modular architecture of a serial-type correlator. It consists of independent analog/random-data converters for the input signals V_1 and V_2 producing corresponding multibit random-data streams $VRD_1(n \cdot \Delta t)$ and

TABLE II
RELATIVE MEAN SQUARE ERRORS OF A RANDOM-DATA CORRELATOR
FUNCTION OF THE NUMBER OF QUANTIZATION LEVELS OF DATA

Quantization levels	Relative mean square error
2	72.23
3	5.75
4	2.75
...	...
8	1.23
...	...
analog	1

$VRD_2(n \cdot \Delta t)$, where Δt is the sampling rate. An r -stage delay line delays by $r \cdot \Delta t$ the second data stream. The multibit multiplier calculates the product $VRD_1(n \cdot \Delta t) \cdot VRD_2((n-r) \cdot \Delta t)$. The resulting stream of product samples is then averaged by the random-data/digital converter, producing an estimation of the correlation function point $COR_{v_1, v_2}(r \cdot \Delta t)$.

Table II gives the performance figures of correlators with different numbers of quantization levels relative to an ideal analog correlator when the inputs are statistically independent Gaussian noise signals with amplitudes restricted within $\pm 3\sigma$ [6]. It can be seen that a basic two-level (1-bit) random-pulse correlator will be 72.23 times slower than an analog correlator, calculating with the same accuracy the correlation function. A three-level correlator will be 5.75 times, and a four-level correlator will be 2.75 times slower than the analog correlator. It can also be seen that by increasing the number of quantization levels from two (as in the case of the random pulses) to three (as in the case of the 2-bit random-data streams), the relative error is reduced by a factor of 12.5.

V. NEURAL-NETWORK ARCHITECTURE USING GENERALIZED RANDOM-DATA REPRESENTATION

Each neuron consists of a number of synapses connected to the neuron body. Each synapse multiplies an incoming signal with a synaptic-stored weight. The weights are adjusted during the learning phase. The neuron body integrates the signals from all the post-synaptic channels. The result of this integration is then submitted to an *activation function* to produce the neuron's output signal.

Fig. 9 shows the random-data implementation of a synapse where the synaptic weights are dynamically stored in an N -stage delay line. Loading weight values from the DATIN input into each register selected by the synapse address SYNADD is done serially when a low logic signal is applied to the control input MODE.

Fig. 10 shows the random-data implementation of a neuron body collecting m random-data streams $DT_{ij} = X_i^* w_{ij}$ from all the incoming post-synaptic channels. The results of this addition are then integrated by a moving-average random-data/digital converter. Since the neuron output will be used as a synaptic input to other neurons, a final digital/random-data converter stage is used to restore the randomness of Y_j .

Because of the functional similarity of a neuron and a correlator, we based our decision about the NN architectural complexity on the performance figures given in Table II. We have opted for the NN architecture using a three-level (2-bit)

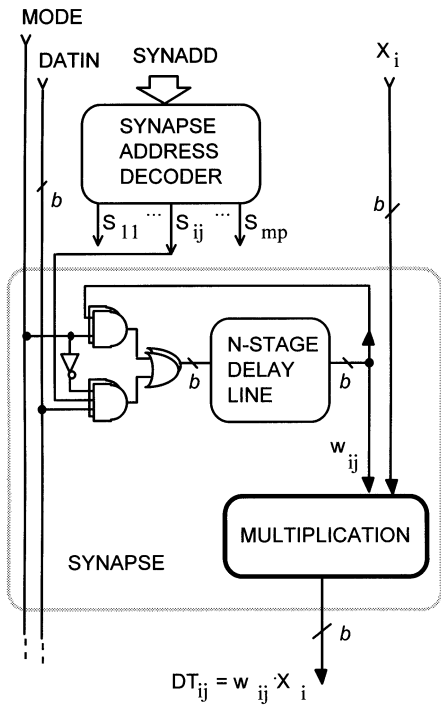


Fig. 9. Multibit random-data implementation of a synapse.

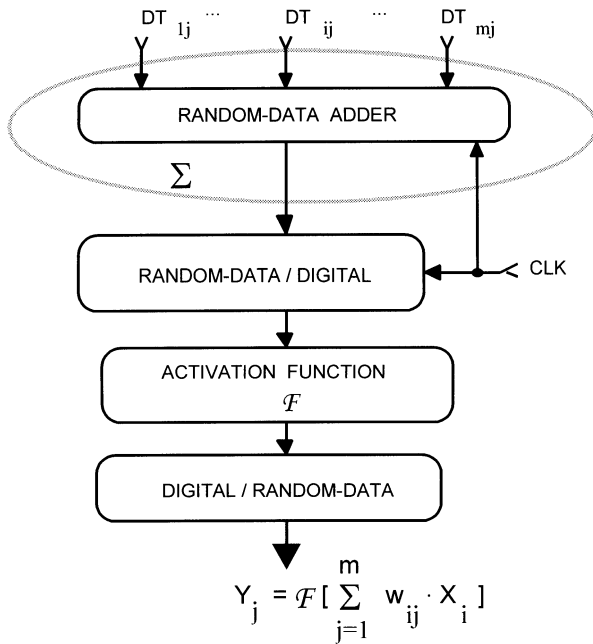


Fig. 10. Multibit random-data implementation of a neuron body.

random-data representation, which gives a good tradeoff between the processing speed and the circuit complexity [6] and [26].

As an example, we have implemented an auto-associative memory using a 2-bit random-data representation, shown in Fig. 11.

Auto-associative memory NNs can learn input-pattern/target $\{P_q, t_q\}$ associations: $\{P_1, t_1\}, \{P_2, t_2\}, \dots, \{P_Q, t_Q\}$.

After training, this NN is able to recognize any of the initially taught associations: if it receives an input $P = P_q$ then it produces an output $a = t_q$, for $q = 1, 2, \dots, Q$. Furthermore, it can

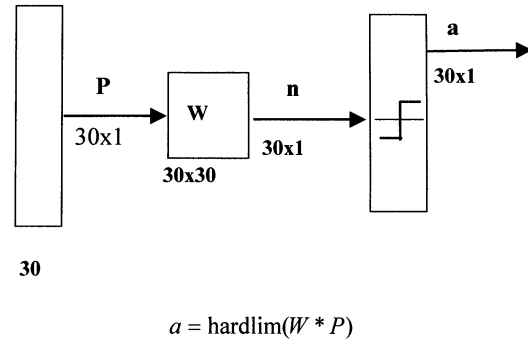


Fig. 11. Auto-associative memory NN architecture.

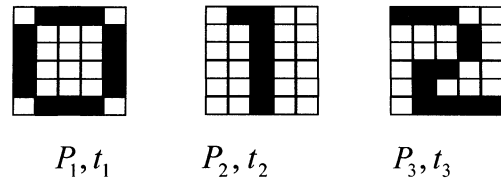


Fig. 12. Training set for the auto-associative memory.

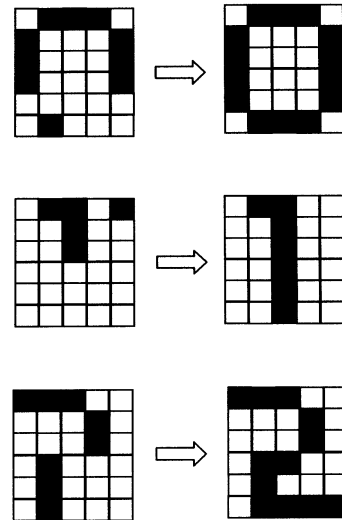


Fig. 13. Recovery of 30% occluded patterns.

recognize patterns corrupted by noise: i.e if the input is changed $P = P_q + \delta$ the output will still be $a = t_q$.

The patterns used for recognition, Fig. 12, represent the digits $\{0, 1, 2\}$ displayed in a 6×5 grid. Each white square is represented by a “-1”, and each black square is represented by a “1.” To create the input vectors, we scan each 6×5 grid one column at a time. The weight matrix in this case is

$$W = P_1 P_1^T + P_2 P_2^T + P_3 P_3^T. \quad (8)$$

In addition to recognizing all the patterns of the initial training set, the auto-associative NN is also able to deal with up to 30% noise-corrupted patterns as illustrated in Fig. 13.

VI. CONCLUSION

Due to their minimal data processing complexity and inherent high internal noise immunity, random-pulse machines represent

an attractive alternative to the analog techniques for many statistical signal processing and NN applications. Because the information is carried internally by sequences of pulses (i.e., by 1-bit data streams), these machines take a relatively long time to produce results with an acceptable accuracy. In order to reduce this processing time, the paper proposes a multibit stochastic machine architecture where the information is carried by multibit data streams.

In order to decide on the optimal number of bits for the internal data representation, one needs to solve a classical time-versus-complexity tradeoff depending on the specific intended application, as well as on the type and cost of the employed technology. However, it is quite apparent that, compared with the commonly used random-pulse representation, the 2-bit random-data representation offers a remarkable speed increase in reaching a desired accuracy at the price of a relatively modest increase in circuit complexity.

REFERENCES

- [1] J. von Neuman, "Probabilistic logics and the synthesis of reliable organisms from unreliable components," in *Automata Studies*, C. E. Shannon, Ed. Princeton, NJ: Princeton Univ. Press, 1956.
- [2] W. J. Poppelbaum and C. Afuso, "Noise-computer," Univ. Illinois, Urbana, Dept. Computer Science, Quart. Tech. Progress Rep., Jan.–Mar. 1965, Apr.–June 1965, July–Sept. 1965, Jan.–Mar. 1966.
- [3] S. T. Ribeiro, "Random-pulse machines," *IEEE Trans. Electron. Comp.*, vol. EC-16, pp. 261–276, June 1967.
- [4] B. R. Gaines, "Stochastic computer thrives on noise," *Electronics*, pp. 72–79, July 1967.
- [5] SEM—Electronic Correlator, NORMA Messtechnik Tech. Doc.
- [6] K.-Y. Chang and D. Moore, "Modified digital correlator and its estimation errors," *IEEE Trans. Inform. Theory*, vol. IT-16, pp. 699–706, June 1970.
- [7] J. E. Tomberg and K. K. K. Kaski, "Pulse-density modulation technique in VLSI implementations of neural network algorithms," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1277–1286, May 1990.
- [8] A. Hamilton, A. F. Murray, D. J. Baxter, S. Churcher, H. M. Reekie, and L. Tarasenko, "Integrated pulse stream neural networks: results, issues, and pointers," *IEEE Trans. Neural Networks*, vol. 3, pp. 385–393, May 1992.
- [9] M. van Daalen, T. Kosel, P. Jeavons, and J. Shawe-Taylor, "Emergent activation functions from a stochastic bit-stream neuron," *Electron Lett.*, vol. 30, pp. 331–333, Feb. 1994.
- [10] E. Petriu, K. Watanabe, and T. Yeap, "Applications of random-pulse machine concept to neural network design," *IEEE Trans. Instrum. Meas.*, vol. 45, pp. 665–669, Apr. 1996.
- [11] L. Schuchman, "Dither signals and their effect on quantization noise," *IEEE Trans. Commun. Technol.*, vol. 12, pp. 162–165, Dec. 1964.
- [12] F. Castanie, "Estimation de moments par quantification a reference stochastique," Ph.D. dissertation, Toulouse, France, 1977.
- [13] —, "Signal processing by random reference quantizing," *Signal Processing*, vol. 1, no. 1, pp. 27–43, 1979.
- [14] E. Pop and E. Petriu, "Influence of reference domain instability upon the precision of random reference quantizer with uniformly distributed auxiliary source," *Signal Processing*, vol. 5, pp. 87–96, 1983.
- [15] J. Vanderkooy and S. P. Lipshitz, "Resolution below the least significant bit in digital systems with dither," *J. Audio Eng. Soc.*, vol. 32, pp. 106–113, 1984.
- [16] M. F. Wagdy and W. Ng, "Validity of uniform quantization error model for sinusoidal signals without and with dither," *IEEE Trans. Instrum. Meas.*, vol. IM-38, no. June, pp. 718–722, 1989.
- [17] M. F. Wagdy, "Effect of various dither forms on quantization errors of ideal A/D converters," *IEEE Trans. Instrum. Meas.*, vol. 38, pp. 850–855, Aug. IM-1989.
- [18] S. P. Lipshitz, R. Wannamaker, and J. Vanderkooy, "Quantization and dither: a theoretical study," *J. Audio Eng. Soc.*, vol. 40, pp. 355–375, 1992.
- [19] R. M. Gray and T. G. Stockham, "Dithered quantizers," *IEEE Trans. Inform. Theory*, vol. 39, pp. 805–912, May 1993.
- [20] M. F. Wagdy and M. Goff, "Linearizing average transfer characteristics of ideal ADC's via analog and digital dither," *IEEE Trans. Instrum. Meas.*, vol. 43, pp. 146–150, Apr. 1994.
- [21] P. Carbone and D. Petri, "Effect of additive dither on the resolution of ideal quantizers," *IEEE Trans. Instrum. Meas.*, vol. 43, pp. 389–396, June 1994.
- [22] P. Carbone and M. Caciotta, "Stochastic-flash analog-to-digital conversion," *IEEE Trans. Instrum. Meas.*, vol. 47, pp. 65–68, Feb. 1998.
- [23] P. Carbone and D. Petri, "Performance of stochastic and deterministic dithered quantizers," *IEEE Trans. Instrum. Meas.*, vol. 49, pp. 337–340, Apr. 2000.
- [24] A. J. Miller, A. W. Brown, and P. Mars, "Moving-average output interface for digital stochastic computers," *Electron Lett.*, vol. 10, no. 20, pp. 419–420, Oct. 1974.
- [25] A. J. Miller and P. Mars, "Optimal estimation of digital stochastic sequences," *Int. J. Syst. Sci.*, vol. 8, no. 6, pp. 683–696, 1977.
- [26] L. Zhao, "Random Pulse Artificial Neural Network Architecture," M.A.Sc. Thesis, University of Ottawa, Ottawa, ON, Canada, 1998.

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Dr. Das was elected one of the delegates of the prestigious Good People, Good Deeds of the Republic of China in 1981 in recognition of his outstanding contributions in the field of research and education. He is listed in the *Marquis Who's Who Biographical Directory of the Computer Graphics Industry*, Chicago, IL (First Edition, 1984). Dr. Das is the 1996 recipient of the IEEE Computer Society's highest esteemed Technical Achievement Award for his pioneering contributions in the fields of switching theory and modern digital design, digital circuits testing, microarchitecture and microprogram optimization, and combinatorics and graph theory. He is also the 1997 recipient of the IEEE Computer Society's Meritorious Service Award for excellent service contributions to IEEE TRANSACTIONS ON VLSI SYSTEMS and the Society, and was elected a Fellow of the Society for Design and Process Science in 1998 for his accomplishments in integration of disciplines, theories and methodologies, development of scientific principles and methods for design process science as applied to traditional disciplines of engineering, industrial leadership and innovation, and educational leadership and creativity.

In recognition as one of the distinguished core of dedicated volunteers and staff whose leadership and services made the IEEE Computer Society the world's preeminent association of computing professionals, he was made a Golden Core Member of the Computer Society in 1998. He is also the recipient of the IEEE Circuits and Systems Society's Certificates of Appreciation for services rendered as Associate Editor of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, from 1995–1996 and 1997–1998, and of the IEEE Computer Society's Fellow Evaluation Committee, once in 1998, and then in 1999. He serves as a member of the IEEE Computer Society's Fellow Evaluation Committee for 2001, as well. Finally, he is the recipient of the prestigious Rudolph Christian Karl Diesel Best Paper Award of the Society for Design and Process Science in recognition of the excellence of their paper presented at the Fifth Biennial World Conference on Integrated Design and Process Technology held in Dallas, TX, June 4–8, 2000. He was elected Fellow of the IEEE for his contributions to switching theory and computer design, and is also a member of the IEEE Computer Society, IEEE Systems, Man, and Cybernetics Society, IEEE Circuits and Systems Society, and IEEE Instrumentation and Measurement Society. He is also a member of the ACM.

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Aurel Cornell, photograph and biography not available at the time of publication.