## *CEG 4131 Assignment 2 –Solutions*

1.

- To design a direct network for a 64-node multicomputer, we can use:
  - A 3D torus with 4 nodes along each dimension. The relevant parameters are:
    $d = 3\lfloor r/2 \rfloor = 6$, $D = 3\lfloor r/2 \rfloor = 6$, and $l = 3N = 192$.
    Also $d \times D \times l = 6912$.
  - A 6-dimensional hypercube. The relevant parameters are:
    $d = n = 6$, $D = n = 6$, and $l = n \times N/2 = 6 \times \frac{64}{2} = 192$.
    We have $d \times D \times l = 6912$.
  - A CCC with dimension $K = 4$. The relevant parameters are: $d = 3$, $D = 2K - 1 + \lfloor K/2 \rfloor = 2 \times 4 - 1 + \lfloor 4/2 \rfloor = 9$, and $l = 3N/2 = 96$. The value of $d \times D \times l$ is 2592.

If the quality of a network is measured by $(d \times D \times l)^{-1}$, then a CCC is better than a 3-D torus or a 6-cube. A 3-D torus and a 6-cube have the same quality.

2.

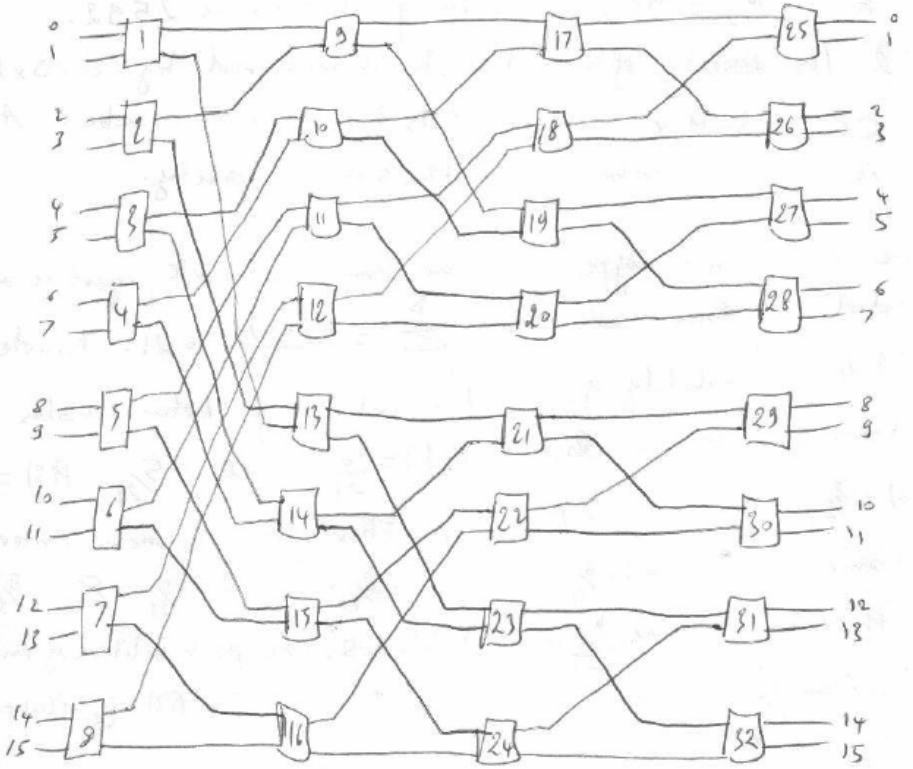
a- For each output terminal, there are 4 possible connections (one from each of the input terminals), so that there are $4 \times 4 \times 4 \times 4 = 256$ legitimate states.

b- $48 = 16 \times 3$ (4×4) switch modules are needed to construct a 64-input Omega network. There are $24 = 4 \times 3 \times 2 \times 1$ permutation connections in a 4×4 switch module. Therefore a total of $(24^{48})$ permutations can be implemented in a single pass through the network without blocking.

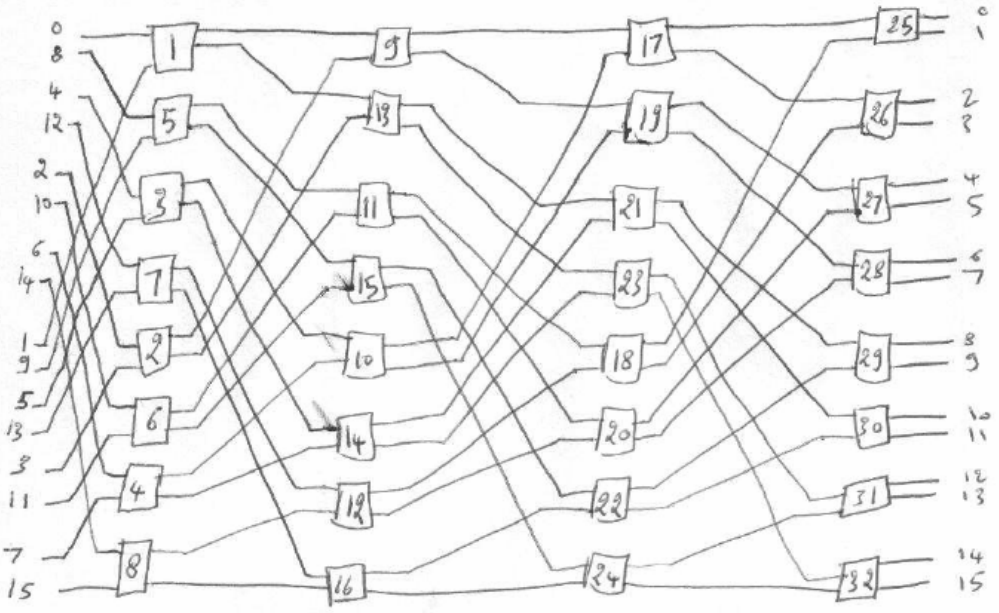
c- The total number of permutations of 64 inputs is 64! so the fraction is $24^{48}/64! \approx 1.4 \times 10^{-23}$.

3.

a- we label the switch modules of a 16x16 Baseline network as below:

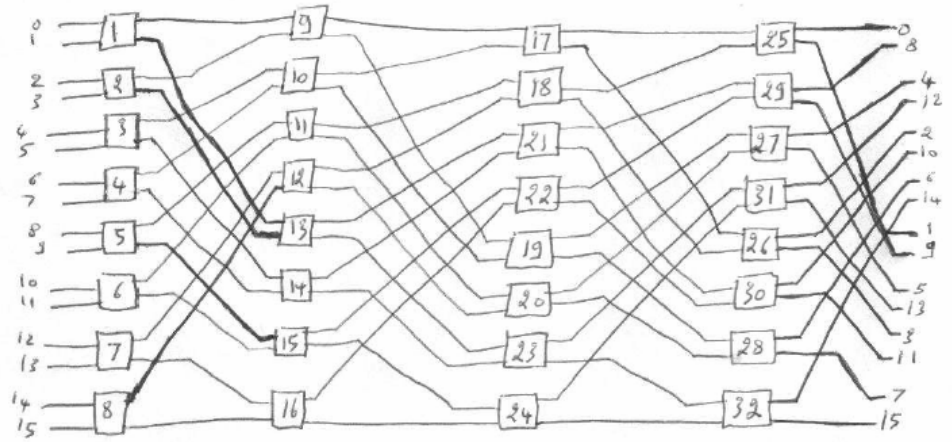



b- Then we change the positions of some switch modules, the Baseline network becomes:




which is just an Omega network.

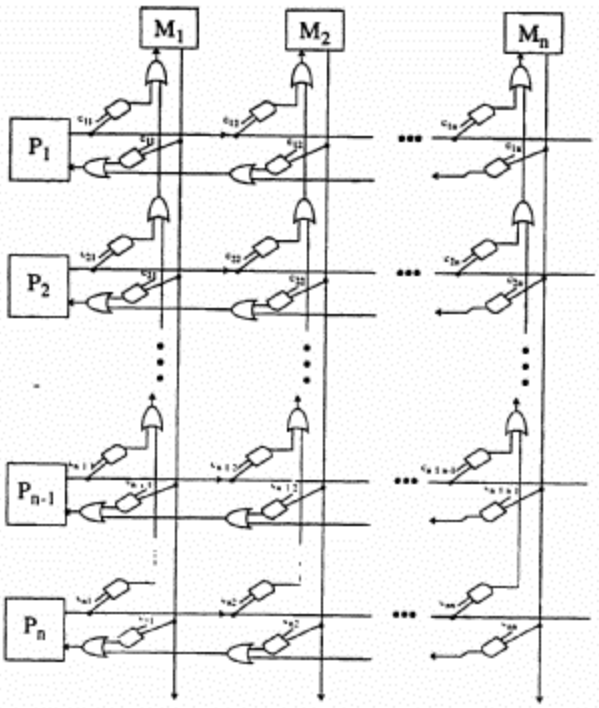
b- IF we change the positions of some switch modules in the Baseline network, it becomes:



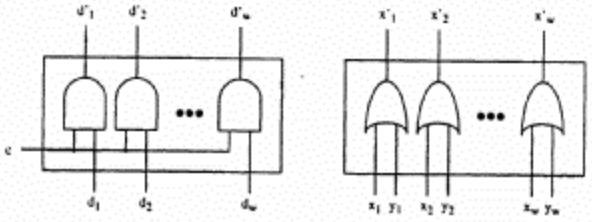

which is just the Flip network.

C- Since both the Omega network and the Flip network are topologically equivalent to the Baseline network, they are topologically equivalent to each other.

4.

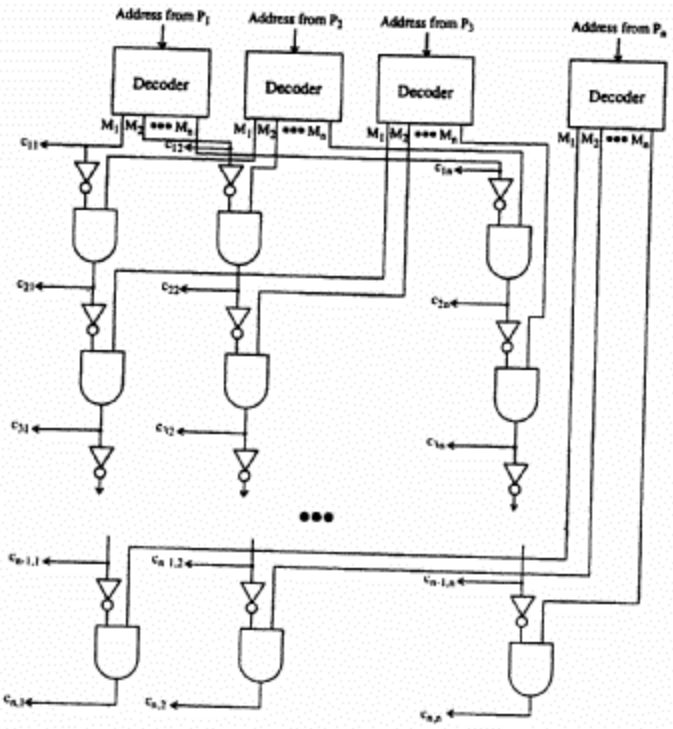



The complexity of the crossbar network can be estimated as follows. At each crosspoint, there are 2 AND gates and 2 OR gates. But in the last row (processor $n$) and last column (memory module $n$), we do not need OR gates for the read/write operation. Therefore, there are $2n^2$ AND gates and $2n^2 - 2n$ OR gates. In practice, each AND or OR gate in the diagram consists of $w$ two-input AND or OR gates as shown in the following diagram.



In total, the number of two-input AND gates is $2n^2w$, and the number of two-input OR gates is $(2n^2 - 2n)w$.

(b) The schematic diagram of the arbiter is shown below:




In case of conflicting requests to access the same memory module, the arbiter will grant priority to the processor with the smallest number. There are $(n-1)$ two-input AND gates along each column, leading to a total requirement of $n(n-1)$ such gates.