CEG 4131 Assignment 1

Problems 1.4, 1.5 and 3.1 from Hwang's book

Problem 1.4 Consider the execution of an object code with 200,000 instructions on a 40-MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment:

Instruction type	CPI	Instruction mix
Arithmetic and logic	1	60%
Load/store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

(a) Calculate the average CPI when the program is executed on a uniprocessor with the above trace results.

(b) Calculate the corresponding MIPS rate based on the CPI obtained in part (a).

Problem 1.5 Indicate whether each of the following statements is *true* or *false* and justify your answer with reasoning and supportive or counter examples:

(a) The CPU computations and I/O operations cannot be overlapped in a multiprogrammed computer.

(b) Synchronization of all PEs in an SIMD computer is done by hardware rather than by software as is often done in most MIMD computers.

(c) As far as programmability is concerned, shared-memory multiprocessors offer simpler interprocessor communication support than that offered by a message-passing multicomputer.

(d) In an MIMD computer, all processors must execute the same instruction at the same time synchronously.

(e) As far as scalability is concerned, multicomputers with distributed memory are more scalable than shared-memory multiprocessors.

Problem 3.1 Consider the parallel execution of the same program in Problem 1.4 on a four-processor system with shared memory. The program can be partitioned into four equal parts (50,000 each) for balanced execution by the four processors. Due to the need for synchronization among the four program parts, 5000 extra instructions are added to each divided program part.

Assume the same instruction mix as in Problem 1.4 for each divided program part. The CPI for the memory reference (with cache miss) instructions has been increased from 8 to 12 cycles due to contentions. The CPIs for the remaining instruction types do not change.

(a) Repeat part (a) in Problem 1.4 when the program is executed on the four-processor system.

(b) Repeat part (b) in Problem 1.4 when the program is executed on the four-processor system.

(c) Calculate the speedup factor of the four-processor system over the uniprocessor system in Problem 1.4 under the respective trace statistics.

(d) Calculate the efficiency of the four-processor system by comparing the speedup factor in part (c) with the ideal case.