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# Digital gamma-ray spectroscopy based on FPGA technology

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## Abstract

A digital pulse processing system convenient for high rate gamma-ray spectroscopy with NaI(Tl) detectors has been designed. The new programmable logic device has been used for implementation of dedicated high-speed pulse processor, as the central part of the system. The processor is capable to operate at the speed of fast ADC, preserving maximum throughput of the system. Special care has been taken to reduce the distortion of energy spectrum caused by pile-up at high-count rates. The developed system is highly flexible, and the parameters of its operation can be changed in software. The performance of the system was tested for high counting rate of  $400\,000\text{ s}^{-1}$ . © 2002 Elsevier Science B.V. All rights reserved.

*Keywords:* Digital pulse processing; Pulse height; Spectroscopy; Pile-up; FPGA devices

## 1. Introduction

The advantages of a digital system for gamma-ray spectroscopy in comparison with a classical analog system are reflected in the possibilities of implementation of complex algorithms and simple modification of algorithms used for signal processing. In this way the highest quality of measurements is achieved both at low and at high counting rates and using various radiation detectors. Other advantages of digital spectrometers, such as simple storage of the spectrum, spectrum processing and analysis and presentation of results, need not be emphasized.

The main functions of a spectroscopy system, such as signal filtering and amplification, pulse pile-up detection and elimination, amplitude analysis and energy spectrum generation, were accomplished through the use of analog and digital circuits of fixed hardware structure in classical systems. In the proposed solution, these functions are implemented by a dedicated DSP with programmable definition of operations. This significantly increases the flexibility of the system, enabling simple reconfiguration and modification of the operation parameters of the system without changing the hardware. Besides, the developed system can simply be linked to a computer or a computer network.

The first digital systems for radiation spectroscopy were implemented by means of standard nuclear instrumentation modules and fast digitizers connected to the computer [1–5]. Also, the programmable logic devices (PLD) and fast TTL

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integrated circuits [6] as well as application specific integrated circuits (ASIC) [7] have been used for digital signal processor design. Standard DSP are commonly used as the main processing element, in some cases along with personal computers [8–11].

In order to achieve acceptable resolution at high counting rates, operating frequency of the signal processor and ADC must be very high (more than 50 MHz). Implementation of the algorithms for pile-up suppression entails several concurrent operations during one clock cycle, which can be obtained only by using dedicated hardware solutions. Digital spectrometers based on standard DSPs can hardly ensure the required signal processing at counting rates above several thousand pulses per second because their architectures are not adapted to this kind of concurrent processing. Insufficient flexibility and high price of ASIC circuits largely discredit this technology in gamma-ray spectroscopy application for high counting rates. Modern field programmable gate arrays (FPGA), thanks to their flexible internal structure and the possibility for the designer to define and change the function of the circuit by programming, represent a very good choice in realization of dedicated DSP in gamma-ray spectroscopy.

In this paper, FPGA technology is applied in realization of a pulse processor for high counting rate gamma-ray spectroscopy with NaI(Tl) detector. The pulse processor is linked to a personal computer that enables display and storage of the spectrum.

## 2. Method description

The main concept in the realization of the system is that the entire signal processing and pulse high analysis has to be accomplished digitally. The only analog parts in the system are a fast amplifier and a base line restorer, which are placed between detector and ADC. The amplifier is used to adjust the signal from the detector to the ADC input. Because base line is not constant in the system due to the changes of temperature and counting rate, a simple circuit for base-line stabilization has been used.

Within the digital pulse processor, by application of a set of algorithms on digital samples, the effect of noise and the probability of pulse pile-up are reduced, pulse pile-up is detected, pulse amplitude is determined and energy spectrum is generated. In order to improve processing for high counting rate, great emphasis is put on the algorithm for pile-up elimination or rejection. The mentioned algorithm begins with clipping of the digitized pulse from the NaI(Tl) detector in order to reduce the probability of pulse pile-up which is proportional to the pulse width. Pulse clipping is achieved subtracting from the original anode pulse its delayed and attenuated fraction. This can be represented by the following expression:

$$V_0(nT) = V_i(nT) - k \cdot V_i(nT - n_1T), \quad (1)$$

where  $T$  is the ADC sample period and operating period of digital pulse processor,  $V_i(nT)$  is the input samples from the detector at the discrete time instant  $nT$ ,  $kV_i(nT - n_1T)$  is the input samples attenuated  $k$  times ( $0 < k < 1$ ) and delayed in time for the fixed interval  $n_1T$ ,  $V_0(nT)$  is the output clipped samples at the discrete time instant  $nT$  used for further processing.

The clipped anode pulses have roughly Gaussian pulse shape. They are characterized by approximately equal duration of leading and trailing edge and constant width (if there is no pile-up), measured just above the base line of the signal. The width of the clipped pulse  $T_p$  is defined as the sum of the delay of the attenuated fraction of the original anode pulse  $n_1T$  and duration of leading edge of the pulse  $t_1$ ,

$$T_p = n_1T + t_1. \quad (2)$$

If the interval between neighboring pulses exceeds the width of the clipped pulse  $T_p$ , they can be separated and their amplitudes will be correctly registered. Fig. 1a shows an example of a digitized anode pulse from NaI(Tl) detector which contains two piled-up pulses. These pulses are separated using the digital clipping techniques (Fig. 1b).

If the interval between neighboring pulses is less than the width of the clipped pulse  $T_p$ , the resulting clipped pulse will be wider  $T_r > T_p$ ,

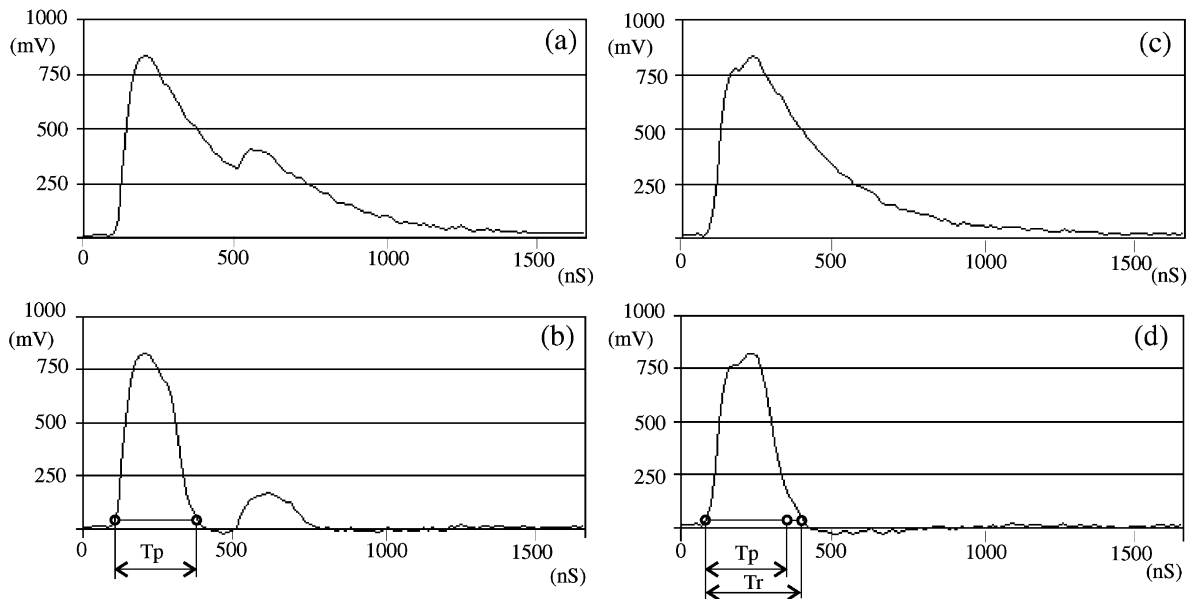


Fig. 1. An example of a digital anode signal from NaI(Tl) detector which contains two pulses (a). These pulses are separated by application of the clipping techniques (b). An example of pile-up that occurred in the region of the leading edge of the pulse is given in (c). The resulting pulse  $T_r$  is wider than the clipped individual pulse  $T_p$  (d) which is used in pile-up detection.

and such wider pulses are rejected. Pile-up detector is used to measure the width of clipped pulses and to estimate if the pulses should be rejected or not. An example of pulse pile-up that occurs on the pulse leading edge is presented in Fig. 1c. The resulting clipped pulse is wider than the individual pulse (Fig. 1d), which means that pile-up detector will conclude that pile-up has occurred.

The pulse amplitude is determined by integration of digital samples that belong to a single clipped pulse. In this way the effect of the quantization noise is reduced as well as that of differential nonlinearity of ADC [8,12]. For these reasons ADC requirements in a digital system are less strict than those in a classical analog system, both in terms of resolution (number of bits) and of differential nonlinearity.

The amplitude distribution of registered pulses is temporarily stored in the local memory of the DSP. This data is periodically transferred to the personal computer, which is used for on-line display and permanent storage of the energy spectrum.

### 3. Realization of the system

The central point and the most critical part of the system because of the requirement for high frequency implementation is the digital pulse processor. The main role of the processor is the application of the algorithm described in the previous chapter for clipping pulses, pile-up detection and rejection at a frequency of 60 MHz. The total system throughput is mainly determined by operation speed of the digital pulse processor. The other functions like energy spectrum generation and communication with the PC which donot require such a high frequency for their processing are implemented in software by using a general purpose DSP. A general-purpose microprocessor could be used instead. A block diagram of a realized system is shown in Fig. 2.

The incoming pulses from the NaI(Tl) detector are fed into a fast operational amplifier.<sup>2</sup> Use of a base-line stabilization block is optional and can be included as a preprocessing element.

<sup>2</sup>AD8041 by Analog Devices.

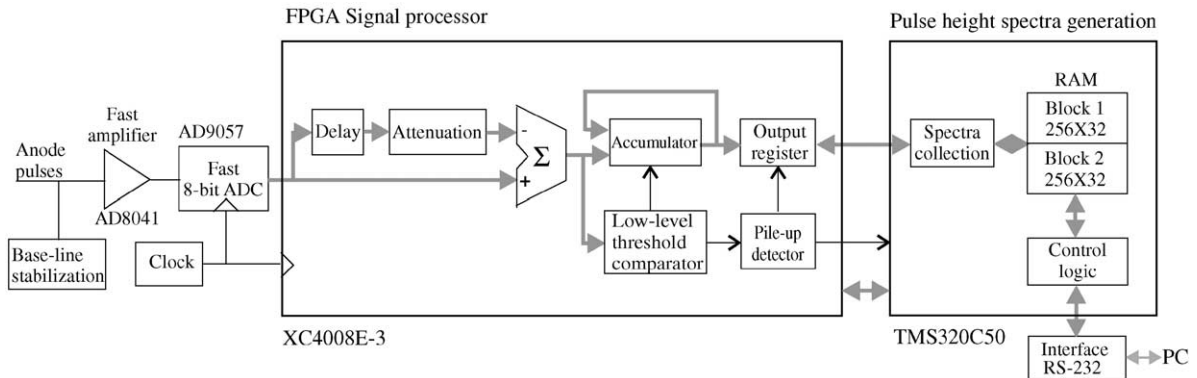


Fig. 2. Block diagram of the digital pulse processing spectrometer based on FPGA device.

The amplified signal is converted into digital samples by means of a CMOS pipe-line ADC,<sup>3</sup> which operates at the rate of 60 MHz and has 8-bit resolution. Low power consumption and a very reasonable price characterize this ADC.

Fast digital signal processing is carried out by a FPGA device<sup>4</sup> [13]. A general purpose digital signal processor (DSP)<sup>5</sup> is used for pulse height spectrum generation, temporary storage, counting rate measurement as well as communication with the personal computer.

The pulse processor performs low-pass filtering, digital pulse clipping, detection of pile-up and integration of digital samples in order to determine the pulse amplitude. Only those pulses with amplitude above the threshold level are registered. The pile-up detector permits writing the result of integration of data into the output processor register and signals to the DSP that the integration result is ready to be read in case when no pulse pile-up is detected.

In the DSP, based on the pulse amplitude, the proper memory location is accessed and its content is incremented. In this way the energy spectrum is formed and temporarily stored in the DSP memory. The spectrum is alternately formed in one of the two memory blocks. While the spectrum

is stored in one block, the data are sent from the other to the PC where they are displayed and permanently stored. For generation of a spectrum with the resolution of 256 channels,  $256 \times 32$ -bit memory blocks have been used.

In order to develop the algorithm for signal processing at the rate of 60 MHz in real-time, it was necessary to design complex functions such as attenuation block, programmable delay block and high-speed accumulator. The first is implemented as a high-speed multiplier with constant coefficients. Using the macro blocks of XC4000E series and pipe-line approach, the accumulator and the multiplier were designed to operate at the speed of 75 and 66 MHz, respectively. FIFO memory based on dual-port RAM with programmable depth, which is related to the time constant  $n_1$ , is used for realization of delay block.

The personal computer program was developed by use of software package for virtual instrumentation<sup>6</sup> [14]. This program enables the transfer of energy spectrum blocks from the pulse processor to the personal computer as well as display and storage of the spectrum. Using this program, the user can change operating parameters of the pulse processor such as threshold level, level of the width of the pulses in the pile-up detection block  $T_p$ , multiplication coefficients  $k$  and time delay  $n_1$ .

<sup>3</sup>AD9057 by Analog Devices.

<sup>4</sup>XC4008E-3 by Xilinx.

<sup>5</sup>TMS320C50 by Texas Instruments.

<sup>6</sup>LabWindows/CVI by National Instruments.

#### 4. Results

The operating characteristics of the implemented digital spectrometer system were tested at low and very high counting rates using radiation sources of different energy. A  $75\text{ mm} \times 75\text{ mm}$  NaI(Tl) detector was used in all experiments. Energy resolution measurements were performed at low counting rates by means of sources  $^{137}\text{Cs}$ ,  $^{60}\text{Co}$  and  $^{232}\text{Th}$ . Results of these measurements are presented in Table 1, in the table the results of measurements with the same detector, but obtained by application of a classical spectrometer system, are shown for comparison.

Based on results from Table 1 it can be concluded that a digital spectrometer has a slightly lower energy resolution in comparison with a classical analog spectrometer. This is due to a relatively low resolution and speed of operation of the used ADC which are limited to 8 bits and 60 MHz, respectively.

The performance evaluation at high counting rates was done using a low activity  $^{232}\text{Th}$  source in the presence of  $^{137}\text{Cs}$  of very high activity. The total counting rate in this experiment was  $400\,000\text{ s}^{-1}$ . The spectrum obtained is marked by

Table 1

Resolution of a digital spectrometer system and a classical spectrometer for different sources of radiation by NaI(Tl) detector at low counting rates

Source	Energy resolution (%)	
	Digital spectrometer	Classical spectrometer
$^{137}\text{Cs}$	7.5	6.8
$^{60}\text{Co}$	5.6	5.1
$^{232}\text{Th}$	4.7	4.2

the symbol ( $\blacktriangle$ ) in Fig. 3. In order to estimate the efficiency of the applied algorithm of digital signal processing the experiment was repeated, with the system reconfigured in order to operate without pulse shortening and without pile-up detection. The energy spectrum obtained in this condition is marked by ( $\blacksquare$ ) in Fig. 3. A degradation due to pulse pile-up is clearly visible. In the same figure, the symbol ( $\blacklozenge$ ) mark  $^{232}\text{Th}$  spectrum measured at low counting rates when the effects of pile-up can be neglected.

By comparison of the spectrum obtained at low counting rates with the ones obtained at very high counting rates it can be concluded that due to

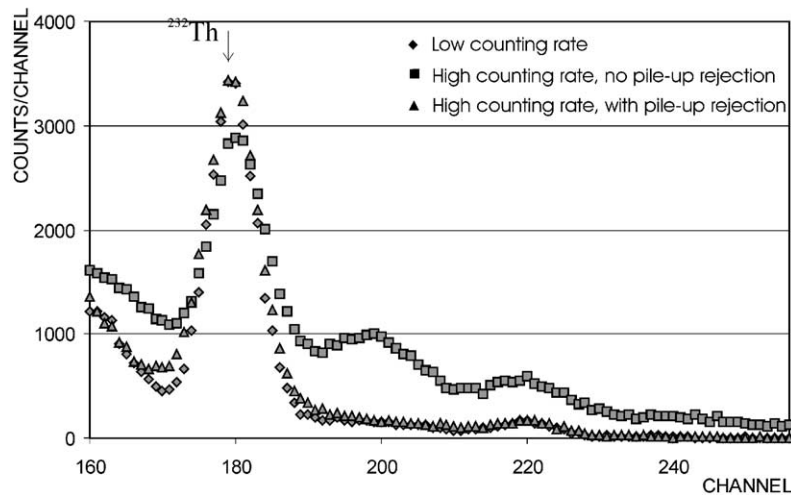


Fig. 3. ( $\blacktriangle$ ) The spectrum of  $^{232}\text{Th}$  in the presence of  $^{137}\text{Cs}$  at high counting rates of  $400\,000\text{ p/s}$ , when pulse shortening is applied and pulse pile-up detected and eliminated. ( $\blacksquare$ ) Spectrum of  $^{232}\text{Th}$  in the presence of  $^{137}\text{Cs}$  at high counting rates of  $400\,000\text{ p/s}$  without pile-up reduction by means of pulse shortening and without detection and elimination of pulse pile-up. ( $\blacklozenge$ ) Spectrum of  $^{232}\text{Th}$  at low counting rates.

application of the described digital procedure of signal processing, the effect of pile-up on energy resolution is strongly reduced.

## 5. Conclusion

The paper describes the principle of operation and the development of a completely digital spectrometer system with a NaI(Tl) detector suitable for high-quality gamma-ray spectroscopy at very high counting rates. The central part of the system, the high-speed parallel pulse processor, is realized using a FPGA device. Deployment of such a specific processor makes it possible to implement digital signal processing algorithms for pulse shortening, pile-up detection and determination of pulse amplitude in real-time. In view of the fact that the processor operates at the speed of ADC, maximum throughput of the system is achieved. The number of analog circuits is reduced to the minimum, because the whole processing is accomplished in digital domain.

The possibility of reprogramming and flexibility are significant characteristics of the developed system. Due to these characteristics, in the evaluation of system characteristics, it was possible to implement different algorithms for signal processing without changing the hardware. It is important to note that these changes can be introduced quickly and while the system is in exploitation. This property of the system is extremely significant when measurements are performed with a large number of detectors. In such cases manual adjustment of system parameters is very time consuming and prone to errors.

It is necessary to stress that, due to the simple structure of the system and low cost of the components used, the total price of the spectrometer, not counting the price of the detector and

the computer, is very low. Performances of the digital spectrometer are directly determined by characteristics of the applied ADC and DSP. The rapid development of technology and architecture of electronic circuits leads to the appearance of increasingly fast digital components of high capabilities, so that increased throughput of the system and higher resolution can be achieved by deployment of faster components but preserving the proposed concept of operation of the system.

## References

- [1] R.E. Chrien, R.J. Sutter, Nucl. Instr. and Meth. A 249 (1986) 421.
- [2] V. Drndarević, P. Ryge, T. Gozani, Nucl. Instr. and Meth. A 277 (1989) 532.
- [3] R. Komar, H. Mak, Nucl. Instr. and Meth. A 336 (1993) 246.
- [4] J.M. Los Arcos, E. Garcia-Torano, Nucl. Instr. and Meth. A 339 (1994) 99.
- [5] W.H. Miller, P. Jackson, C. Lin, Nucl. Instr. and Meth. A 353 (1994) 254.
- [6] V. Jordanov, G. Knoll, IEEE Trans. Nucl. Sci. NS-40 (1993) 764.
- [7] F. Hilsenrath, H.D. Voss, J.C. Bakke, IEEE Trans. Nucl. Sci. NS-32 (1985) 145.
- [8] M. Al-Haddad, C. Lin, W. Miller, R. Berliner, IEEE Trans. Nucl. Sci. NS-41 (1994) 1765.
- [9] P. Simoes, H. Martins, C. Correia, IEEE Trans. Nucl. Sci. NS-43 (1996) 1804.
- [10] B. Simoes, C. Correia, Nucl. Instr. and Meth. A 422 (1999) 405.
- [11] J.M.R. Cardoso, J.B. Simoes, C.M.B.A. Correia, Nucl. Instr. and Meth. A 422 (1998) 400.
- [12] G. Ripamonti, A. Pullia, A. Garaci, IEEE Instrumentation and Measurement Technology Conference, St. Paul, Minnesota, May 18–21, 1998, 666–669.
- [13] Xilinx, The Programmable Logic Company, San Jose, CA, USA, [www.xilinx.com](http://www.xilinx.com).
- [14] National Instrument Corporation, LabWindows/CVI-Visual Programming for Instrumentation, Ver. 3.1, 1995, Austin, TX, USA, [www.natinst.com](http://www.natinst.com).