A Good Method
to Prepare and Use Transparencies
for Research Presentations

Veljko Milutinović
Department of Computer Engineering,
School of Electrical Engineering,
University of Belgrade,
POB 35-54, 11120 Belgrade, Serbia, Yugoslavia

Phone: +381-11-769872, Fax: +381-11-769872
E-mail: vm@etf.bg.ac.yu
WWW: http://galeb.etf.bg.ac.yu/~vm/
Introduction

• Tuning the audience to the subject
• Presenting the forest to the audience
• Preventing misunderstandings of any kind
The Ten Compile-Time Commandments

• Introduction (to tune the reader)
• Problem statement (and why it is important)
• Existing solutions (and their criticism)
• Proposed solution (and its essence)
• Conditions and assumptions (of the analysis to follow)
• Details of the solutions to be compared ($1 + k$)
• Formal analysis (or analytical modeling)
• Simulation analysis (to show performance)
• Implementation analysis (to show complexity)
• Conclusion (from the performance/complexity viewpoint)
The Magnificent Seven

• Elements of the set
• Operations
• Functions
• Axioms
• Lemmas
• Theorem(s)
• Corollaries
Font Size and Line Count: Bad

- Simple superscalar going after high clock rate; four instructions fetching from an 8Kbyte I cache, and placed in one of two I buffers (four instructions in each one).

- Issue goes from the buffers (in-order, no instructions bypassing at all); one must be empty before the other one can be used (simpler design, but slower issue).

- Branches predicted using a 2-bit history table associated within the I cache controller; I issue stalled if 2nd branch encountered before the 1st branch resolved.

- After fetch and decode, instructions are arranged according to the functional unit they will use; issue follows after the operands are ready (from registers or via bypassing).

- Four FUs: int with shifter, int with branchevalor, FP adder, FP multiplier; integer instructions update registers in-order; FP instructions update files out-of-order; not all FP exceptions are precise.

- On-chip primary caches: 8Kbytes each (I + D, dm for 1cp cache access); a 6-entry MAF with MissAddresses/TargetRegs for up to 21 missed loads (merge).

- On-chip secondary cache: 96Kbytes (shared, 3w/sa); in most of the current microprocessors this cache memory is off the chip.
Font Size and Line Count: Good

- Simple superscalar (four)
- Branch prediction issues (2-bit history table)
- On-chip caches (primary and secondary)

A picture is worth a 1000 words
Automatic Line Breaks: Bad

• Fixed/variable allocation scenarios based on the home property (page manager): DSM + DSIO system approaches
• Writes get satisfied on distance or locally, depending on what brings better performance and smaller complexity
• Good if reads and writes are interleaved with similar probabilities of occurrence
Semantic Line Breaks: Good

• Fixed/variable allocation scenarios based on the home property (page manager): DSM + DSIO system approaches
• Writes get satisfied on distance or locally, depending on what brings better performance and smaller complexity
• Good if reads and writes are interleaved with similar probabilities of occurrence
The Ten Run-Time Commandments

• *Do not hesitate* to redo the presentation desk prior to session start, in order to optimize your efficiency and comfort.
• *Make sure* that you look good during the presentation.
• *Let* the introductory transparency be there while you are being introduced.
• *Check* the screen after each new transparency.
• *Point* at the wall, not at the transparency.
• *Avoid* the SOS words.
• *Watch* your time!!!
• *Remember*, discussion is where you show who you really are.
• *Do not promise*; just suggest the audience to ask by e-mail.
• *Reload* the introductory transparency immediately after you finish.
Conclusion

• Performance versus complexity
• Who will benefit
• Newly open problems…