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# Digital Logic Design: Principles and Practices

ELG5195 (EACJ5705 )  
Carleton CRN: 13040

Winter 2009

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## Schedule:

Monday LEC 19:30-21:00 SITE Room: J0106

Wednesday LEC 19:30-21:00 SITE Room: J0106

Office Hours: Monday, 18:00-19:30

## Course Description

Switching algebra. Combinational circuit design including PLA and VLSI techniques. Special properties-symmetric functions, unate functions, threshold functions, functional decomposition. Sequential circuits-state reduction, incompletely specified machines, state assignments and series-parallel decomposition. Fundamental mode sequential circuits-race, hazards, and state assignment. Semicustom and VLSI design. Special sequential circuits.

## References

1. Randy Katz, Gaetano Borriello, *Contemporary Logic Design*, Pearson – Prentice Hall, 2005, ISBN: 0-201-30857-6
2. Charles H., Jr. Roth, *Fundamentals of Logic Design*, Brooks Cole, 2003, ISBN: 0534378048
3. Donald D. Givone, *Digital Principles and Design*, McGraw Hill, 2003, ISBN: 0072525037
4. Alan B. Marcovitz, *Introduction to Logic Design*, McGraw-Hill, 2001, ISBN: 0071122478
5. *LOGIC DESIGN*, Editor-in-Chief Wai-Kai Chen, Copyright © 2003 CRC Press, LLC [electronic resource]
6. Rëudiger Ebdndt, Gëorschwin Fey and Rolf Drechsler. Advanced BDD optimization [electronic resource]
7. Zoran Salcic, Asim Smailagic Digital systems design and prototyping using field programmable logic and hardware description languages, [electronic resource]

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## **Marking Scheme**

- 20% Assignments: Two or three assignments, to be handed in during class on the due-date specified.
- 40% A project involving a literature review and some experimental work; a report and a short presentation at the end of the course will be required.
- 40% Final examination
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## **Course Outline**

1. Background for digital design.
2. Logic function representation and minimization.
  - a. Karnaugh maps
  - b. Quine-McCluskey method
  - c. Iterated consensus algorithms
  - d. ESPRESSO minimization algorithms
  - e. Function minimization by using K-map XOR patterns
  - f. Variable-entered K-maps
  - g. Multiple output problems
3. Programmable Logic Devices.
4. Propagation delay and timing defects in combinational logic.
  - a. Static hazards
  - b. Function hazards
  - c. Stuck-at faults and the effect of hazard cover on fault testability
5. Introduction to synchronous state machine design and analysis.
6. Synchronous FSM design considerations and applications.
  - a. State table reduction
  - b. State assignment
  - c. Output race glitches and static hazards
  - d. Asynchronous inputs
  - e. Clock skew
7. Special topics in switching theory
  - a. Threshold logic
  - b. Functional decomposition
  - c. Symmetric functions
8. Alternative Synchronous FSM architectures and systems-level design.
  - a. Algorithmic State Machines
  - b. FSM/ASM realizations using PLA, PAL, ROM, PLD, multiplexers
  - c. FSM architectures centered around a shift register
  - d. FSM architectures centered around a parallel loadable up/down counter
  - e. The One-Hot design method
9. Applications