

**Design Example:** Design an inverting amplifier with a closed loop voltage of  $A_v = -5$ . Assume the op-amp is driven by a sinusoidal soorce,  $v_s = 0.1 \sin \omega t$  volts, which has a source resistance of  $R_s = 1 \text{ k}\Omega$  and which supply a maximum current of 5 µA. Assume that the frequency is low.

$$i_S = \frac{v_S}{R_S} (R_S \text{ in this example means two resistances } : R_S = R_1 + R_{ST}.$$

$$R_{SF}$$
 represents the source resistance. Therefore  $i_{S} = \frac{v_{S}}{R_{SF} + R_{I}}$   
If  $i_{S}(\max) = 5\mu A$ , then we write  $R_{I}(\min) + R_{SF} = \frac{v_{S}(\max)}{i_{S}(\max)} = \frac{0.1}{5 \times 10^{-6}} = 20 \text{ k}\Omega$ 

$$R_1$$
 should be 19 k $\Omega$  and  $A_V = \frac{-R_2}{R_{ST} + R_1} = -5.$   
Accordingly  $R_2 = 5(R_{ST} + R_1) = 5 \times 20 = 100 \text{ k}\Omega$ 

## To Solve Ideal Op-Amp Circuit

- If the noninverting terminal of the op-amp is at ground potential, then the inverting terminal is at virtual ground. Sum currents at this point, assuming zero current enters the op-amp itself.
- If the noninverting terminal of the op-amp is not at ground potential, then the inverting terminal voltage is equal to that at the noninverting terminal. Sum currents at the inverting terminal node, assuming zero current enters the op-amp itself.
- For an ideal op-amp circuit, the output voltage is determined from either step 1 or step 2 above and is independent of any load connected to the output terminal.

## Amplifier with a T-Network



Combing the above equations we get

$$A_{\mathcal{V}} = \frac{v_O}{v_S} = -\frac{R_2}{R_1} \left(1 + \frac{R_3}{R_4} + \frac{R_3}{R_2}\right) \qquad 4$$

**Design Example:** An op-amp with a T-network is to be used as a preamplifier for a microphone. The maximum microphone output voltage is 12 mV (rms) and the microphone has an output resistance of 1 k $\Omega$ . The op-amp circuit is to be designed such that the maximum output voltage is 1.2 V (rms). The input amplifier resistance should be fairly large but all resistance values should be less than 500 k $\Omega$ .

$$|A_{\mathcal{V}}| = \frac{1.2}{0.012} = 100$$

$$A_{\mathcal{V}} = -\frac{R_2}{R_1} (1 + \frac{R_3}{R_4}) - \frac{R_3}{R_1}$$
If we choose  $\frac{R_2}{R_1} = \frac{R_3}{R_1} = 8$ 

$$-100 = -8(1 + \frac{R_3}{R_4}) - 8; \frac{R_3}{R_4} = 10.5$$

We should include the value of the source resistance in the calculation

If we set  $R_1 = 49 \text{ k}\Omega$  and  $R_{\text{sr}} = 1 \text{ k}\Omega$  then the total resistance ( $R_1 \text{ effective}$ ) will be 50 k $\Omega$  $R_2 = R_3 = 400 \text{ k}\Omega$  and  $R_4 = 38.1 \text{ k}\Omega$ 

#### **A Single Difference or Differential Amplifier**



6

#### **Instrumentation Amplifier**

#### Input (a) and output (b) stages of Instrumentation amplifier



$$A_{V} = \frac{v_{out}}{v_{1} - v_{2}} = \frac{R_{F}}{R} \left( 1 + \frac{2R_{2}}{R_{1}} \right)$$

7

(b)

**Design Example:** Determine the range required for resistor  $R_1$  in the instrumentation amplifier to realize a differential gain adjustable from 5 to 500. Assume  $R_F = 2R$ , so that the difference amplifier gain is 2.

• Assume  $R_1$  is a combination of a fixed resistor  $R_{1f}$  and a variable resistor  $R_{1v}$ . Assume  $R_{1v} = 100 \text{ k}\Omega$ 

$$A_{V} = \frac{v_{out}}{v_{1} - v_{2}} = \frac{R_{F}}{R} \left( 1 + \frac{2R_{2}}{R_{1}} \right)$$

$$500 = 2 \left( 1 + \frac{2R_{2}}{R_{1f}} \right) \text{ and the minimum differential gain is}$$

$$R_{1v}$$

$$5 = 2 \left( 1 + \frac{2R_{2}}{R_{1f} + 100} \right) \text{ and from the maximum gain expression}$$

$$2R_{2} = 249R_{1f}$$

$$1.5 = \frac{2R_{2}}{R_{1f} + 100} = \frac{249R_{1f}}{R_{1f} + 100}$$

$$R_{1f} = 0.606 \text{ k}\Omega \text{ and } R_{2} = 75.5 \text{ k}\Omega$$

## Large Signal Operation of Op Amp

- Like other amplifiers, op amps operate linearly over a limited range of output voltages.
- Another limitation of the operation of op amps is that their output current is limited to a specified maximum. For example, the op amp 741 is specified to have a maximum output current of  $\pm 20$  mA.
- Read Example 2.5.
- Another phenomenon that can cause nonlinear distortion when large output signals are present is that of slew-rate limiting. This means there is a specific maximum rate of change possible at the output of a real op amp. This maximum is known as the slew rate (SR) of the op amp and is defined as

$$SR = \frac{dv_O}{dt} \bigg|_{max}$$

**Design Example.** Design a difference amplifier with a specified gain and minimum differential input resistance. Design the circuit such that the differential gain is 30 and the minimum differential input resistance is  $R_i = 50 \text{ k}\Omega$ 

> $R_{i} = 2R_{1} = 50 \text{ k}\Omega$   $R_{1} = R_{3} = 25 \text{ k}\Omega$ Since the differential gain is  $\frac{R_{2}}{R_{1}} = 30$ , we must have  $R_{2} = R_{4} = 750 \text{ k}\Omega$

# **DC Imperfections** Offset Voltage

- The IC Op-amp comes so close to ideal performance that it is useful to state the characteristics of an ideal amplifier without regard to what is inside the package.
  - Infinite voltage gain
  - Infinite input impedance
  - Zero output impedance
  - Infinite bandwidth
  - Zero input offset voltage (exactly zero out if zero in).

- Build any op amp circuit, apply zero voltage to its input, and what do you expect at the output?
- Although you would zero voltage, there is actually an error voltage present at its output.
- What causes this error? You can trace the error back to a number of unbalances in the op amp's internal transistors and resistors. To account for this in a circuit design, the net error is **modeled** as an offset voltage,  $V_{OS}$ , in series with op amp's input terminals.
- How will it affect the circuit? That depends on the op amp itself and the circuit design.

- The input offset voltage can range from  $\mu V$  to mV and can be either polarity.
- Bipolar op amps have lower offset voltages than JFET or CMOS types.
- The offset voltage is modeled in series with one of the op amp input terminals. Which one?
- Although the net effect is the same at either input, it is much easier to analyze V<sub>OS</sub> in series with the non-inverting input. Why? The resulting circuit with V<sub>OS</sub> at V+ looks just like the non-inverting amplifier configuration.



- In many applications, especially those for which the input signal is large compared to the offset voltage  $V_{OS}$ , the effect of the offset voltage is negligible.
- However, there are situations in which it is necessary to compensate for or null out the offset voltage.
- Two such methods are:
  - Offset null terminals: Some op amp are provided with two additional terminals to which a specified circuit can be connected to trim to zero the output DC voltage due to  $V_{OS}$ .
  - Offset compensation circuit through two terminals.
  - Capacitively coupling the amplifier.



The output DC offset voltage of an op amp can be trimmed to zero by Connecting a potentiometer to the two offset-nulling terminals. The wiper Of the potentiometer is connected to the negative supply of the op am.



Capacitively coupled inverting amplifier.

**Exercise 2.24:** Consider an inverting amplifier with a nominal gain of 1000 constructed from an op amp with an input offset voltage of 3 mV and with output saturation levels of  $\pm 10$  V. (a) What is the peak sine-wave input signal that can be applied without output clipping? (b) If the effect of  $V_{OS}$  is nulled at room temperature (25 oC) how large an input can now one apply if: (i) the circuit is to operate at a constant temperature? (ii) the circuit is to operate at a temperature in the range 0°C to 75 °C and the temperature coefficient of  $V_{OS}$  is 10  $\mu$ V/°C?

$$V_o = V_{OS} \left(1 + \frac{R_2}{R_1}\right); V_o = 3 \text{mV}(1 + 1000) = 3 \text{V}$$

Maximum amplitude of a sine wave at the op amp output is 10 - 3 = 7V. (b) For part (i) = 10 mV

(b) For part (ii) : Temperature range of  $0^{\circ}$  C to  $75^{\circ}$  C corresponds to input offset voltage range of  $(0-25) \times 10 \mu V = -250 \mu V$  to  $((75-25) \times 10 \mu V = 500 \mu V)$ . This input offset range corresponds to output DC levels of  $-250 \mu V (1+1000) = -0.25 V$  to  $500 \mu V (1+1000) = 0.5 V$ . **Exercise 2.25:** Consider an inverting amplifier with a nominal gain of 1000 constructed from an op amp with an input offset voltage of 3 mV and with output saturation levels of  $\pm 10$  V. The amplifier is capacitively coupled. (a) What is the DC offset voltage at the output and what is the peak sine wave signal that can be applied at the input without output clipping? Is there a need for offset trimming? (b) If  $R_1 = 1$  k $\Omega$  and  $R_2 = 1$  M $\Omega$ , Find the value of *C* that will ensure that the gain will be greater than 57 dB down to 100 Hz.

The maximum amplitude of a sine wave at the output without clipping is 10 - 0.3 mV = 9.997 V, accordingly there is no need for offset trimming.

(b) The magnitude of the gain of this amplifier is  $|A_d| = \frac{R_2}{|R_1 + \frac{1}{i\omega c}|} = \frac{R2}{\sqrt{R_1^2 + \frac{1}{c^2\omega^2}}}$ 

$$\frac{20 \log |A_d| > 57; |A_d| > 707.95;}{\sqrt{R_1^2 + \frac{1}{c^2 \omega^2}} > 707.95; C = 1.59 \mu F}$$

# • One of the practical op timp initiations is that the input bias currents for the two inputs may be slightly different.

- Even though the inputs are designed to be symmetrical, slight differences which occur in the manufacturing process may give slightly different bias currents.
- This offset current is typically on the order of a tenth of the input bias current, with 10 nA being a representative offset current for a 741 op amp.
- Even with identical source impedances, this offset current will produce a slight voltage between the input terminals, contrary to the ideal op amp.



$$R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

 $V_o = I_{OS}R_2$  (with  $R_3$ )

- To minimize the effect of the input bias currents one should place in the positive lead a resistance equal to the DC resistance seen by the inverting terminal.
- If the amplifier is AC coupled, we should select  $R_3 = R_2$ .
- We must always provide a DC path between each of the input terminals of the op amp and ground. If we couple both input of the amplifier then the circuit will not operate without the resistance  $R_3$  to ground.

**2.26:** Consider an inverting circuit designed using an op amp and two resistors,  $R_1 = 10 \text{ k}\Omega$  and  $R_2 = 1 \text{ M}\Omega$ . If the op amp is specified to have an input bias current of 100 nA and an input offset current of 10 nA, find the output DC offset voltage resulting and the value of resistor  $R_3$  to be placed in series with the positive input lead in order to minimize the output offset voltage. What is the new value of Vo.

$$V_{O} = I_{B}R_{2} = 100 \text{ nA} \times 1 \text{ M}\Omega = 0.1 \text{ V}$$
$$R_{3} = \frac{R_{1}R_{2}}{R_{1} + R_{2}} = 9.9 \text{ k}\Omega \approx 10 \text{ k}\Omega$$
$$V_{O} = I_{OS}R_{2} = 10 \text{ nA} \times 9.9 \text{ kA} \approx 0.01 \text{ V}$$